DESIGN OF COMPACT ON-CHIP FILTERS FOR RF FREQUENCIES

B.TECH PROJECT
REPORT

SUBMITTED FOR THE PARTIAL
FULFILLMENT OF
THE DEGREE OF
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ABSTRACT

Use of spiral inductors for the design of adaptive equalizers for RF frequencies consume large amount of chip area. Here, design methodologies have been discussed which can potentially reduce the chip area by around 50%. Based on the ideas, adaptive equalizers for 6.25Gb/s have been designed and layed out for fabrication.

Optimization techniques for the design of compact on-chip low pass filters have been discussed.

1. INTRODUCTION

The theory of passive element filters was mainly developed during 1970s. But for on chip design, passive elements are too bulky for below RF frequency. But as the frequency increases, the value of the passive elements scales down. At RF/Microwave frequencies, passive elements are small enough to be realized on chip. At these high frequencies, anyway the amplifier based circuits give bad performance.

The inductors on chip even at RF occupy large area. Moreover inductors should be kept far apart on chip to avoid inter-inductor coupling. The distance between two inductors is generally comparable to the size of inductors themselves as the magnetic coupling decays very slowly. This is not a problem with capacitors as the capacitive coupling decays much faster.

The aim of this project is to find a way to design circuits at RF frequencies using this magnetic coupling as a circuit element.

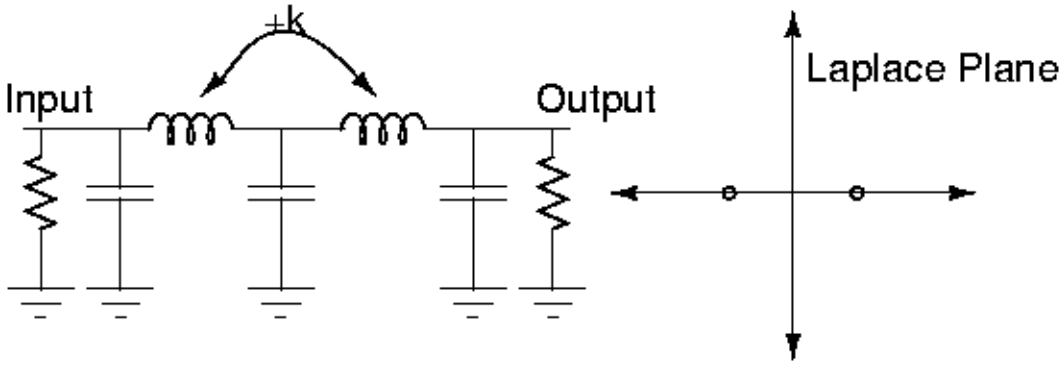
2. THEORY

There is a vast literature on passive filter design. But even after a extensive survey, filter design using positive magnetic coupling was not found. A few designs, like elliptic filter, using negative magnetic coupling exist. But negative coupling decreases the total inductance so is not very preferable. Also positive coupling can be realized very easily by winding spiral inductor.

2.1 ANALYSIS OF COUPLED LC LADDER

Analysis of simple LC ladders with positive magnetic coupling introduced between inductors give following results.

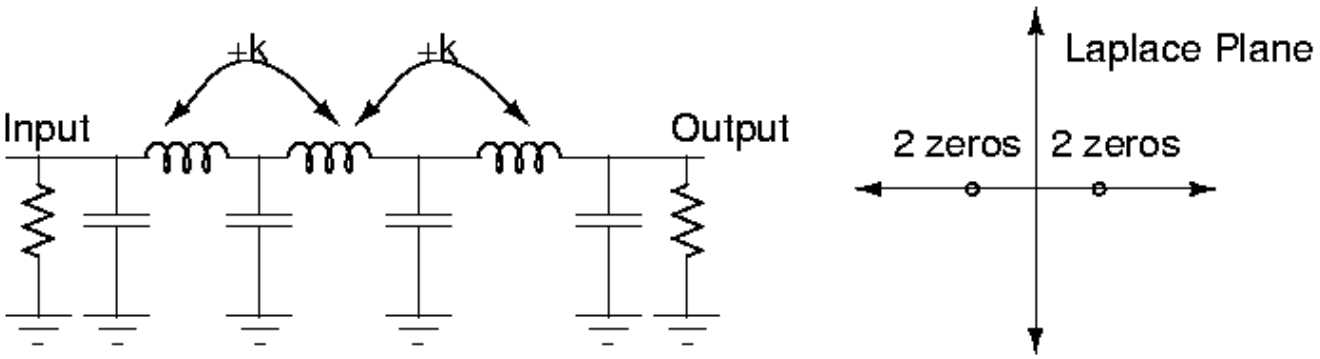
--- A ladder with two positively coupled inductors has zeros on the real axis(Fig 1).



(a) (b)

Fig 1: (a) 5th order system with coupled inductors
(b) Real axis zeros

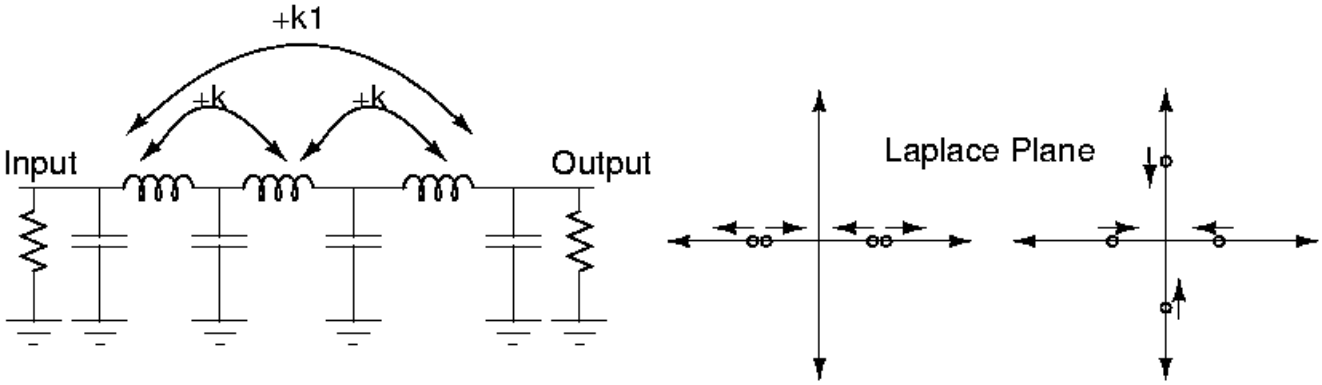
--- If a ladder with three inductors is considered in which only adjacent inductors are positively coupled, the ladder has four zeros on the real axis. If the value of all the inductors and coefficient of couplings is same, the zeros overlap on the real axis(Fig 2).



(a) (b)

Fig 2: (a) 7th order system with coupled inductors
(b) zeros on the real axis

Now if positive coupling(k1) is introduced between the first and the last inductors, the zeros split. As this coupling increases, the zeros move farther from each other in different directions(Fig 3b). If coupling increases beyond a certain value, two of the four zeros shift to the imaginary axis(Fig 3c).



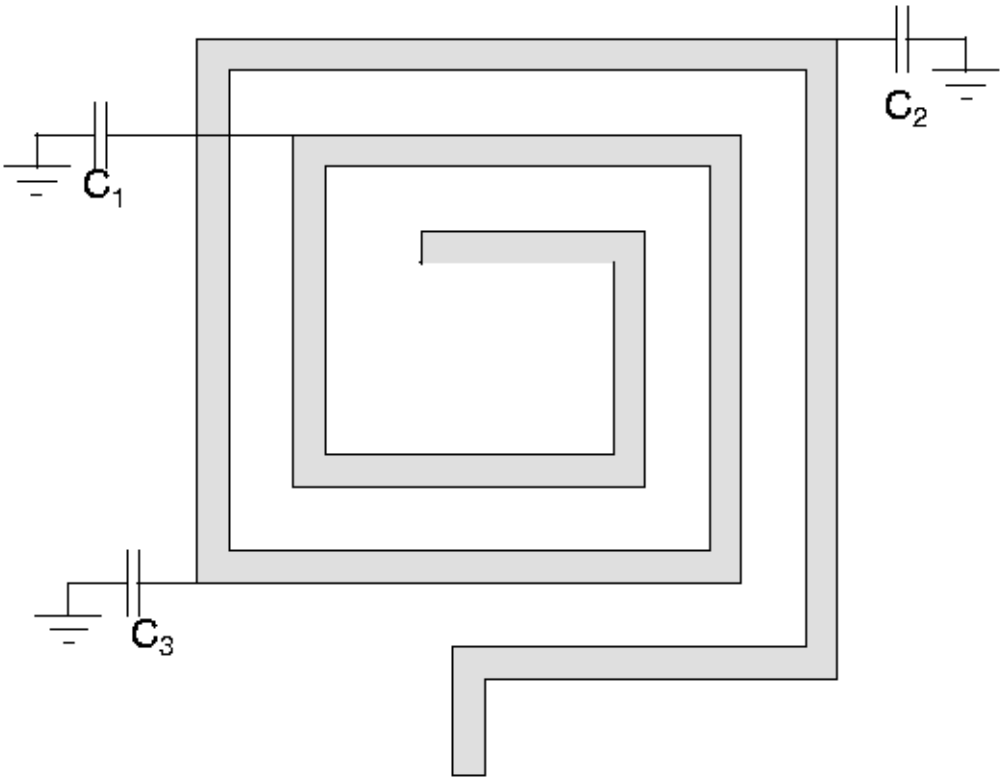
(a) (b) ©

Fig 3: (a) 7th order system with coupled inductors
(b) Movement of zeros as k1 increases
© Movement of zeros as k1 increases further

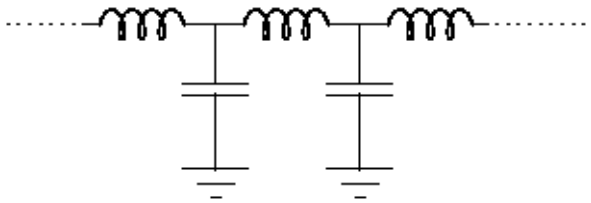
--- As the order of the system increases, poles and zeros move on the s plane with change in coefficients of coupling. Analysis becomes complex, so one has to use optimization for circuit design.

2.2INDUCTOR TAPPING

If an inductor is tapped with capacitors as shown in Fig. 4 , a LC ladder is obtained with all the inductors coupled to each other. Coupling is both capacitive and inductive.



(a)



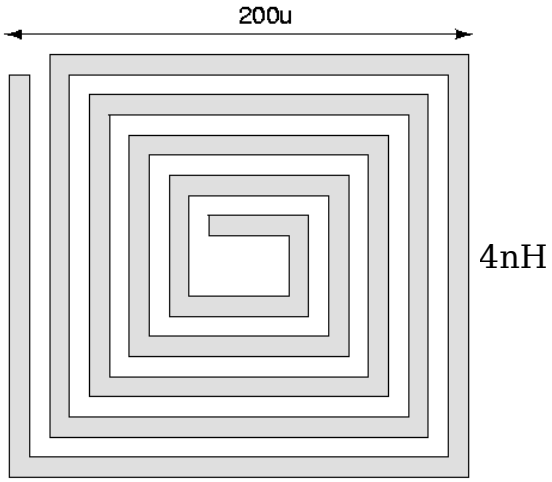
(b)

Fig 4: (a) Tapped inductor
(b) a ladder which can be mimicked

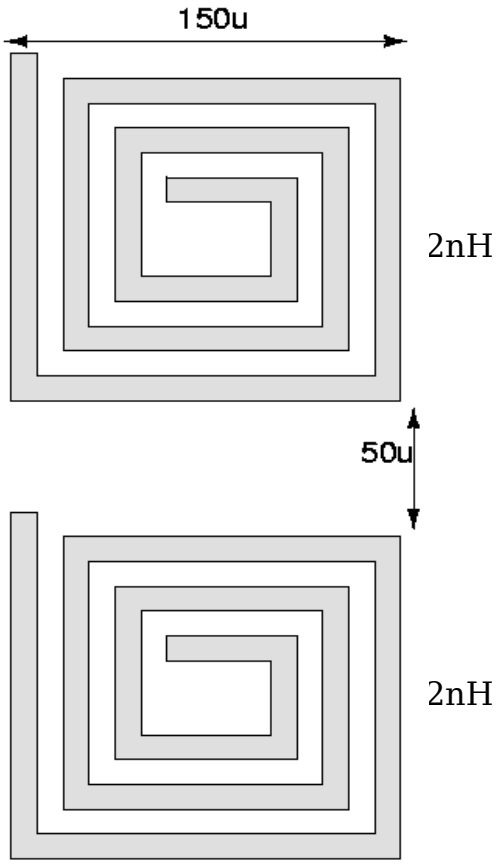
With proper placing of C1, C2, etc. , it is possible to mimic the behavior of

simple LC ladder with more than one inductor. The advantage is that the area can be reduced by a large factor due to following reasons:

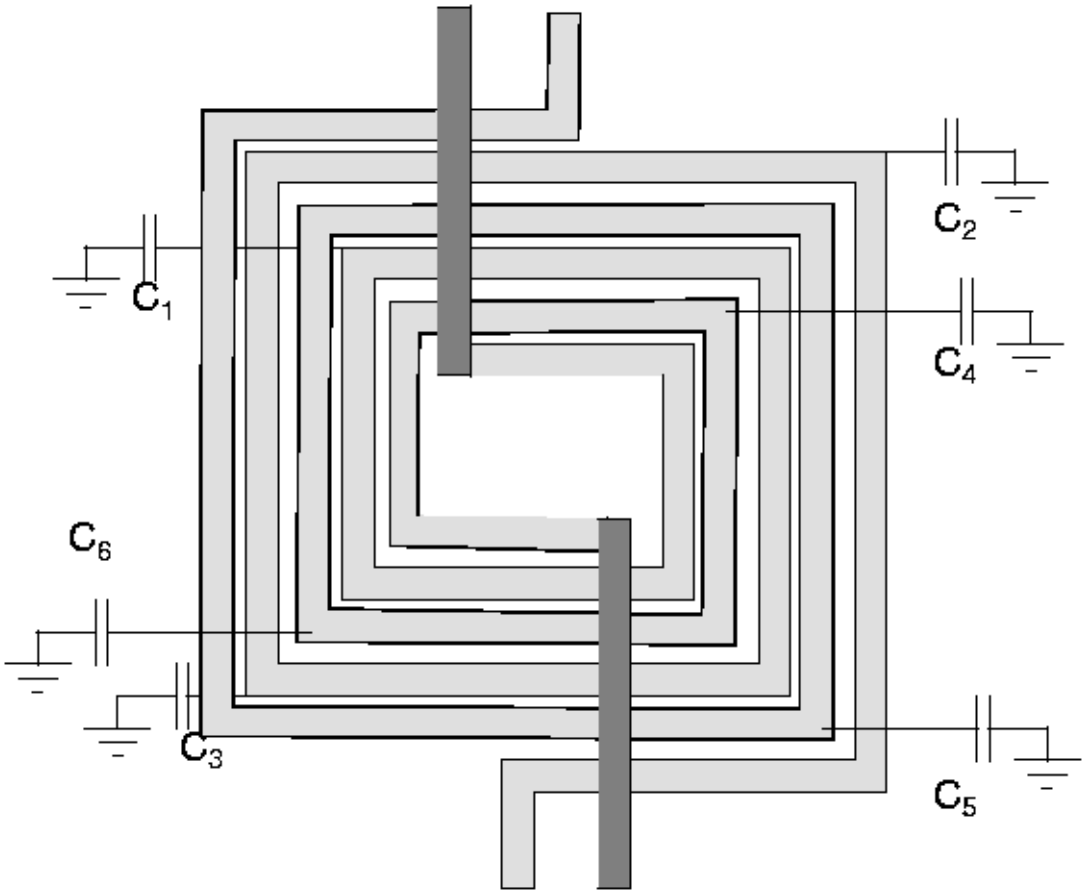
1. Separate inductors will have to be placed far apart to avoid coupling.
2. Suppose there are 2(say) inductors with values L1, L2. If one single inductor of value L1+L2 is realized as a spiral inductor, the area occupied will be lesser than the sum of the area occupied by the 2 inductors as shown below.



200u x 200u = 40000u sq.

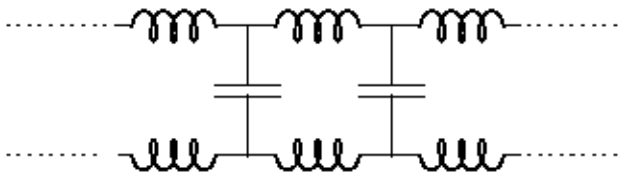


((150u x 2) + 150u) x 150u = 52500u sq.



By similar arguments, it is advantageous to replace a differential LC(Fig 5b) ladder by a differential inductor tapped at appropriate places(Fig 5a) with appropriate amount of capacitance.

(a)



(b)

Fig 5: (a) A tapped differential inductor
(b) A differential ladder which can be mimicked

3 INDUCTOR MODELLING

Fasthenry and fastcap can used to model inductors. Each loop of an inductor can be divided into four segments. Each segment can be treated as a lumped element. Fasthenry was used to extract the inductance and resistance value of each segment. Fastcap can be used to extract the capacitance between each segment and the capacitance between each segment and the ground plate.

3.1 ISSUES IN INDUCTOR MODELLING

3.1.1 Substrate effect

UMC 180 RF/MM provides high resistivity RF substrate. By EM simulations in Microwave Office, it was found that if the substrate to ground contact is 75 u away from the ground, the inductor capacitance to the ground can be neglected.

3.1.2 Proximity of ground line to the inductor

Inductor will couple with any signal ground line running close to it. By EM simulations, it was observed that if the horizontal distance between the inductor and any ground line on metal1 or metal2 is more than 50u, then the effect if not significant.

3.1.3 Dependence of Inductor parameters on frequency

The frequency dependence of the inductance and resistance due to skin effect and proximity effect was not modeled. But the variation in inductance and resistance with frequency was observed in fasthenry and then the design was simulated with these variations. There was no significant difference. Anyway, it was observed that the skin effect is most dominant from 7 to 8 GHz which is

out of the range of interest. The additional resistance due to proximity effect at 10GHZ was found to 0.01% of the total resistance, so proximity effect can be safely neglected.

The inter-loop capacitance has a frequency dependence effect on the response. But this effect was neglected in the modeling.

3.2 MODELLING

For modeling a non-differential inductor, a inductor is divided in several segments as showh in Fig 6.

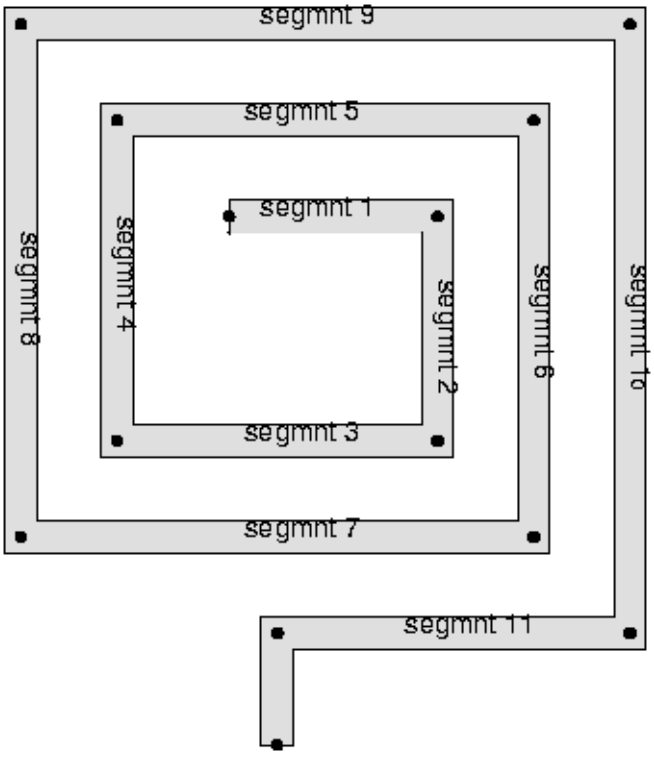
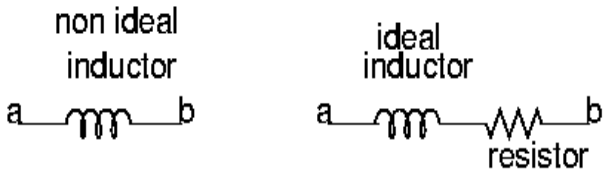


Fig 6: Division of an inductor in segments
Corners of the inductors have been marked by dots

For simplicity of figures, series resistance has not been explicitly indicated in any models below. Every inductor should be viewed as a non-ideal inductor(Fig 7a) which can be modeled as in Fig 7b.



(a) (b)

Fig 7: (a) non-ideal inductor
(b) modeling of the non-ideal inductor

Each segment is treated as a lumped inductor as shown in Fig. 8 (for simplicity capacitance between far apart nodes have not been shown)

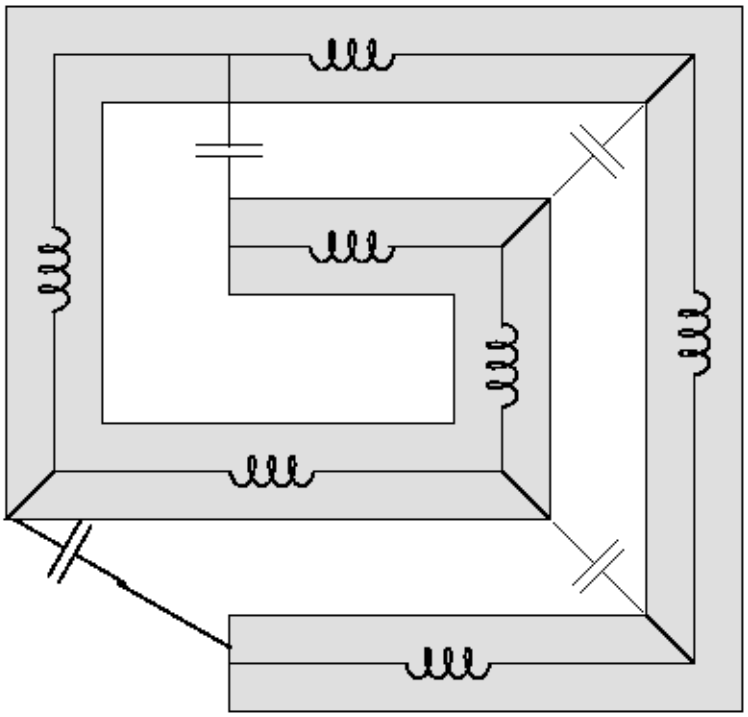


Fig 8: Treatment of each segment as a lumped element

A very exact modeling will look as in Fig. 9 (for simplicity only four segments have been considered).

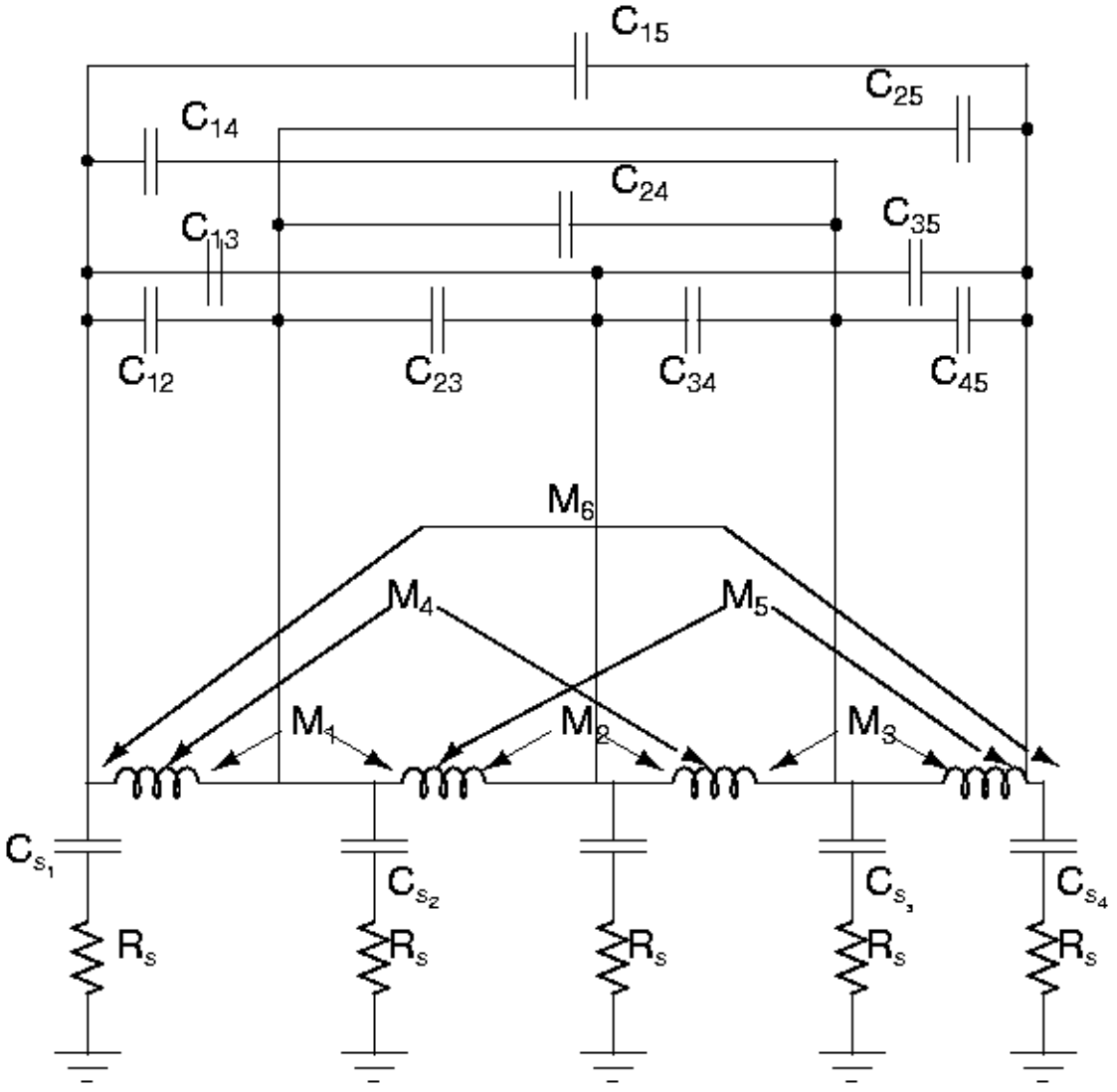


Fig 9: Inductor Modeling

But as discussed in 3.1.1, substrate resistors and capacitors can be neglected. As C13, C24, C35, C14, C25, C15 will be negligible compared to C12, C23, C34, C45(Fig 10), they can be neglected. Thus the modeling reduces to as shown in Fig. 11.

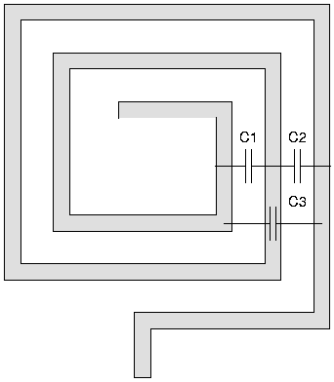


Fig 10: It can be seen from this figure that C3 is negligible compared to C1 and C2

For more accuracy, these capacitors can be retained. But in some technologies, the passivation layer on the top metal layer is so complex can it make not be possible to model inter-loop capacitance using fastcap. UMC 180 RF/MM has such a complex passivation. But then, such technologies provide, capacitance tables which can be used to model C1 and C2 but not C3.

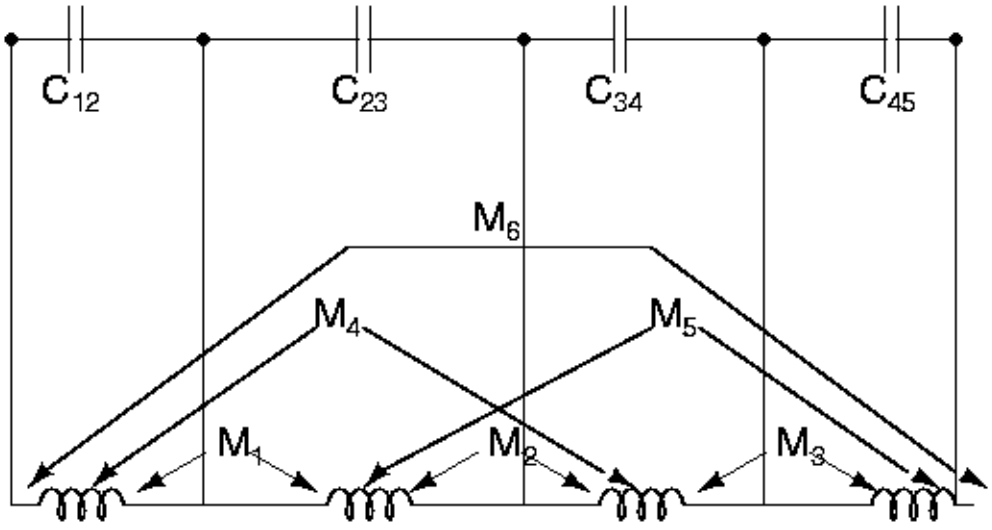
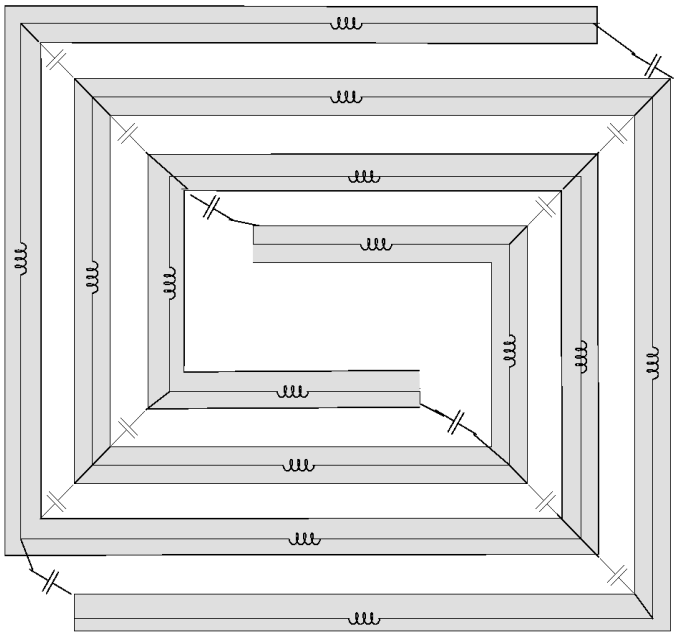
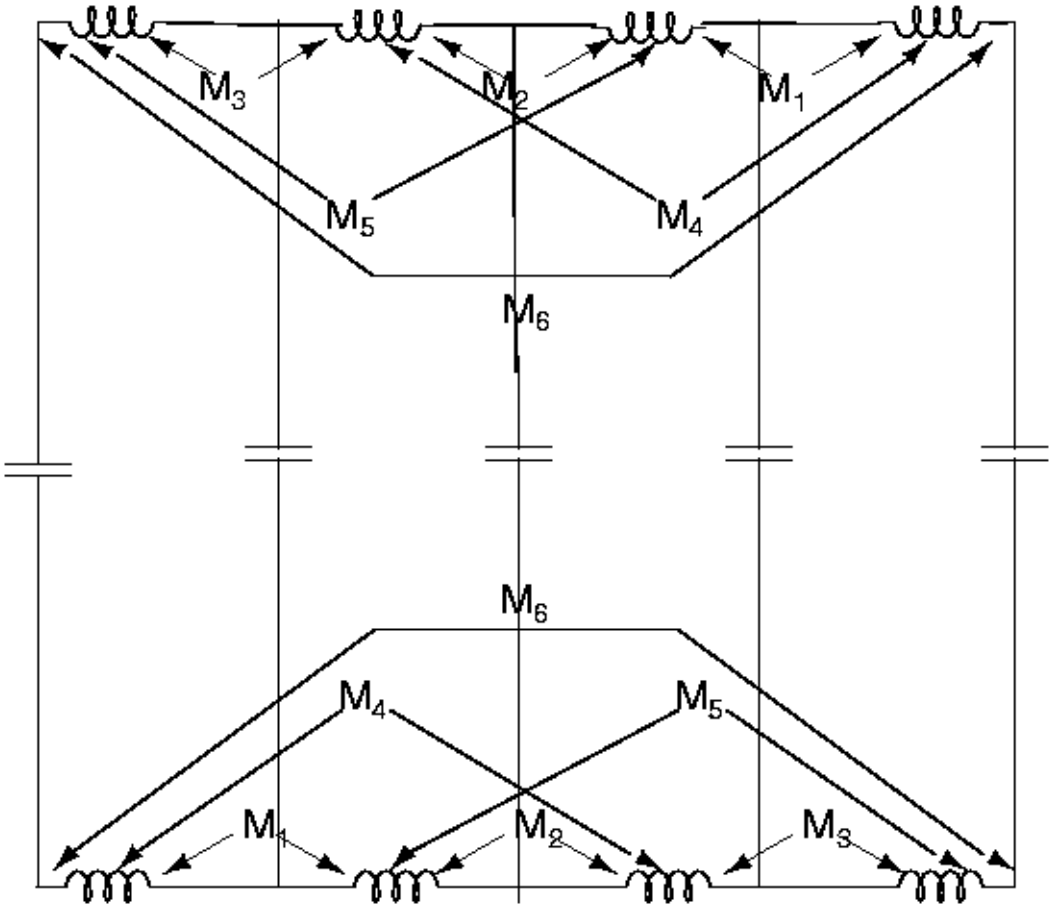


Fig 11: Simplified modeling of inductor

Following the similar arguments,a differential inductor can be modeled as in Fig.



(a)



(b)

Fig 12: (a) Treatment of each segment of the differential inductor as a lumped inductor
(b) Model for a differential inductor

4 OPTIMIZATION

Matlab was used for optimization. Here the idea is to optimize capacitance from the corners of the inductor or an array of inductors to the ground to obtain the desired circuit behavior.

Given the value of inductor, inter-loop spacing and width of conductor, matlab routine can create an inductor using fasthenry. Then it extracts the parameters of the inductor using both fastcap and fasthenry. Initial value of the capacitors between the corners of the inductors and the ground has to be supplied.

Using state space model, the transfer function of the circuit is generated. From the transfer function, various output parameters such as magnitude response, group delay, step response are generated.

Matlab function 'fgoalattain' is used for optimization. It requires the goals to be achieved as input and tries to minimize the difference between the goals and the generated response. The group delays required at different taps were given as the goals.

In optimization, initial values of the capacitors to be optimized is important.

The same amount of total capacitance as required in a corresponding LC ladder equalizer divided equally at all the corners of the inductor works very well. After optimization, most of the capacitors reduce to zero. This is good from the design point of view as very few number of capacitors will have to be realized.

5 DELAY LINE FOR TRAVELLING WAVE EQUALIZERS

The topology for a traveling wave equalizer has been shown in Fig. 13.

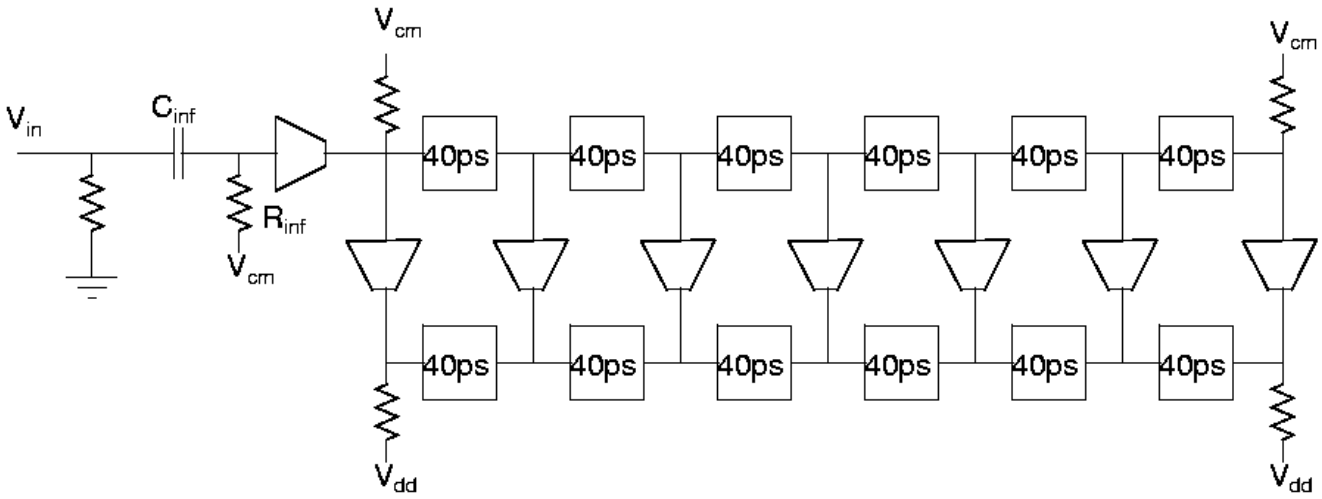


Fig. 13: Traveling Wave Equalizer Topology

A conventional delay line is a LC ladder. For a seven tap traveling wave equalizer, for 6.25Gb/s, each tap gives 40ps of delay. Each tap is realized by cascading two basic cells(Fig. 14).

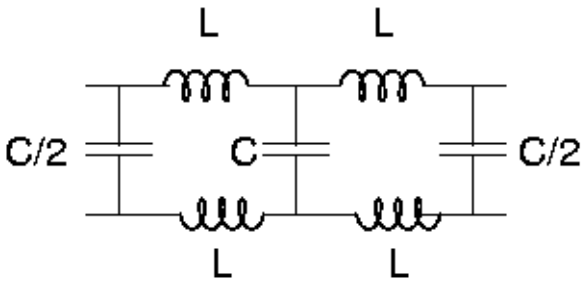


Fig. 14: Basic cell in LC ladder

So, there are two inductors per tap. The two inductors should be kept far apart to reduce the inter-inductor coupling. One solution to this is to use single basic cell per tap but this degrades the performance of the equalizer.

In this project, a methodology has been found by which two basic cells can be replaced by one or less than one basic cell, i.e, each tap can be realized by using one or lesser number of inductors without degrading the performance. Throughout this project report, design examples for 6.25Gb/s traveling wave equalizers will be considered.

6 EQUALIZER WITH DIFFERENTIAL DELAY LINES

6.1 DELAY LINE

The single inductor if optimized for 40ps(say) at the end, the optimized capacitors are on the edges mostly. The group delay obtained can be as accurate as 40.000ps. But when such inductors will be cascaded for the delay line, the response of the inductor at the input also matters. In this case, the group delay response at the input is so bad.

When the optimization is done both at the input and the output, the group delay at the output varies from 38 to 42 ps but the response at the input is good enough for cascading. I this case, the optimized capacitor turns out to be more concentrated at the center of the inductor.

As expected, the bandwidth decreases as the delay to be optimized increases. Individual delay blocks can be cascaded for the entire delay line. But it was found that the performance was much better when the entire delay line is optimized.

Each differential inductor was 4.4nH in value. A transconductance capacitance of 285fF was assumed at all the taps but 1st. At the 1st tap, a trans capacitance of 400fF was assumed. This extra capacitance was included to realize the output capacitance of the input driving transconductance.

For, optimization, equal value of capacitance at all the corners of the six differential inductors was given as the initial value. Then the complete differential delay line was optimized for differential outputs at all the seven taps(Fig. 15) for the frequency range of 0-5GHz. After optimization, only 13

capacitors were found to be non-zero.

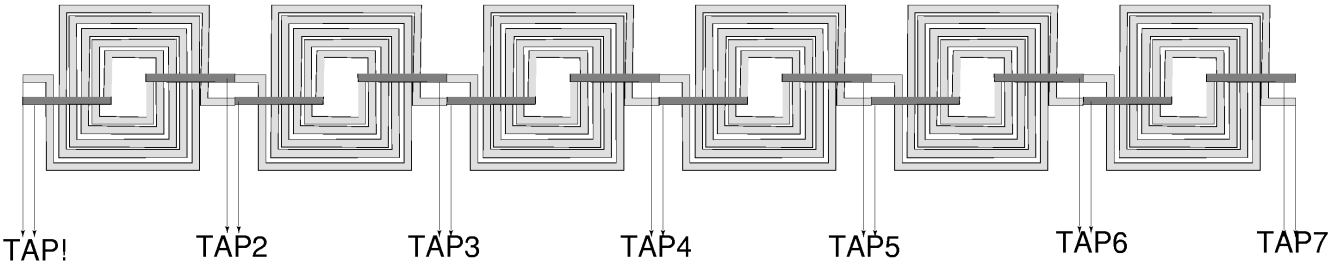


Fig. 15: Delay Line with 7 taps

6.1.1 Design Issues

-- If the inductor is too tight, the capacitance between the differential inductors is too large and there is nothing to optimize. Roughly more that 25% of the required capacitance should be left for optimization. The lesser is the inter inductor capacitance, the better will be the optimized performance.

-- The amount of inductance should be roughly 10% more than the conventional LC ladder design for the total inductor resistance of 40% compared to terminating resistance. More the series resistance, more should be the inductance.

-- Lesser is the range of frequency of optimization, better is the result till the optimized frequency. In the designs presented here, optimization was done till 5GHz.

6.1.2 Advantages

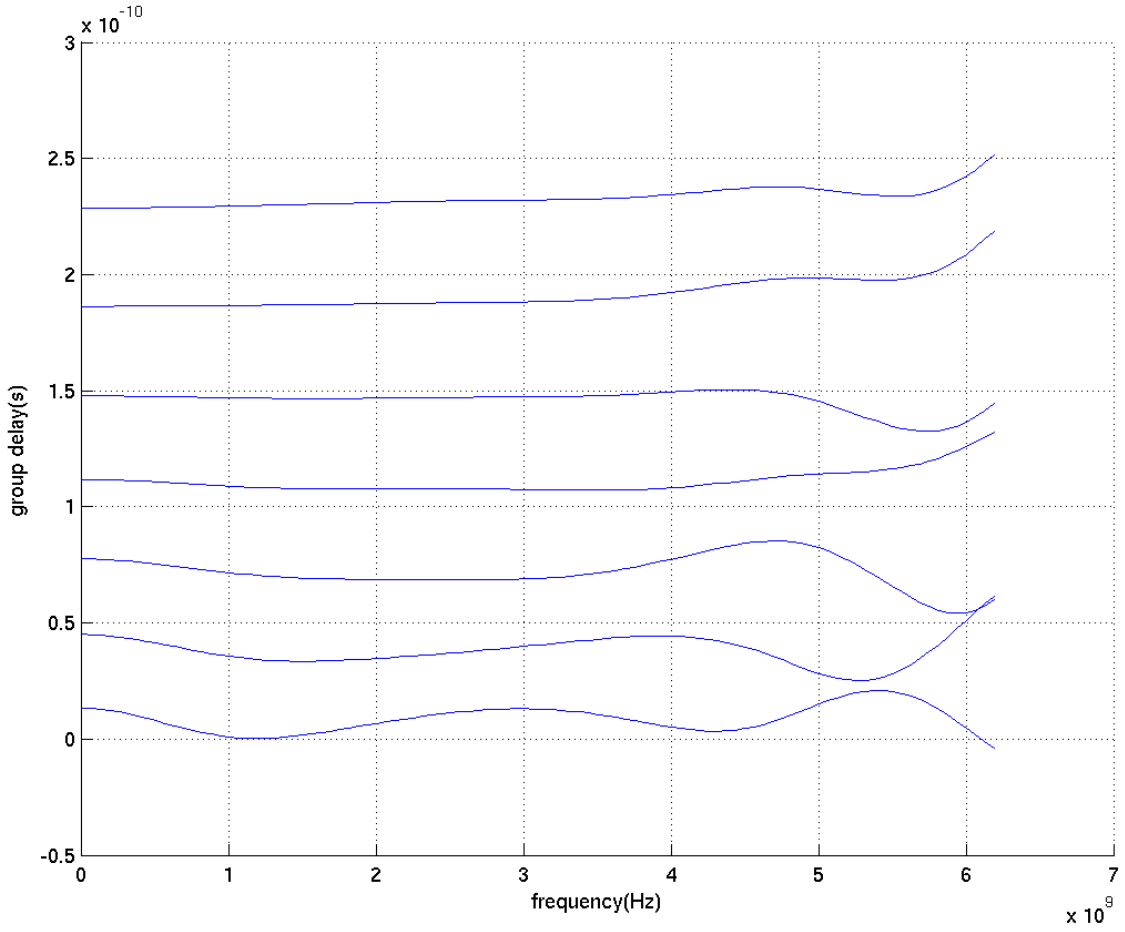
-- In conventional LC ladder, extra inductance has to be added before first tap and after the last tap. In this design there is no such requirement. Even if such a thing is enforced, performance does not improve further.

-- The distance between two inductors can be significantly reduced. The inter-loop magnetic coupling that is thus introduced can be taken care will designing.

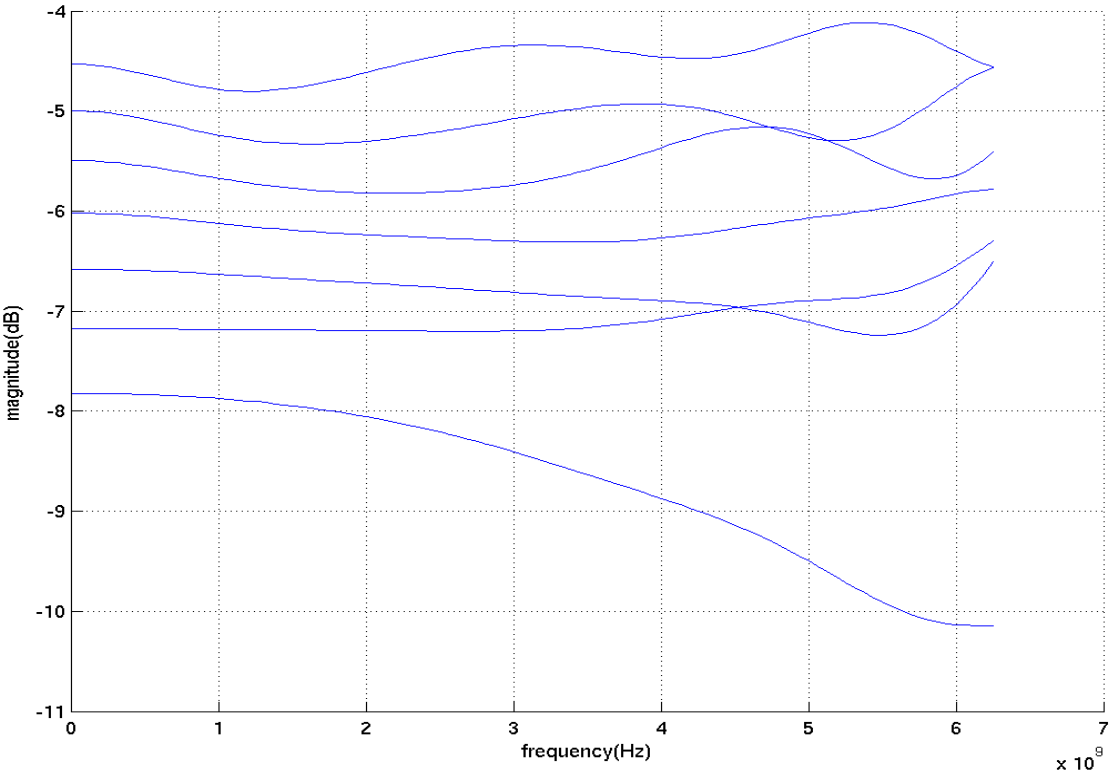
--In the conventional design, the transconductance capacitance has to be same. If it is not the same, extra capacitance is added to make it same. No such constrain is present here. The performance does not depend on the distribution of transconductance capacitance at different taps.

6.1.3 Performance

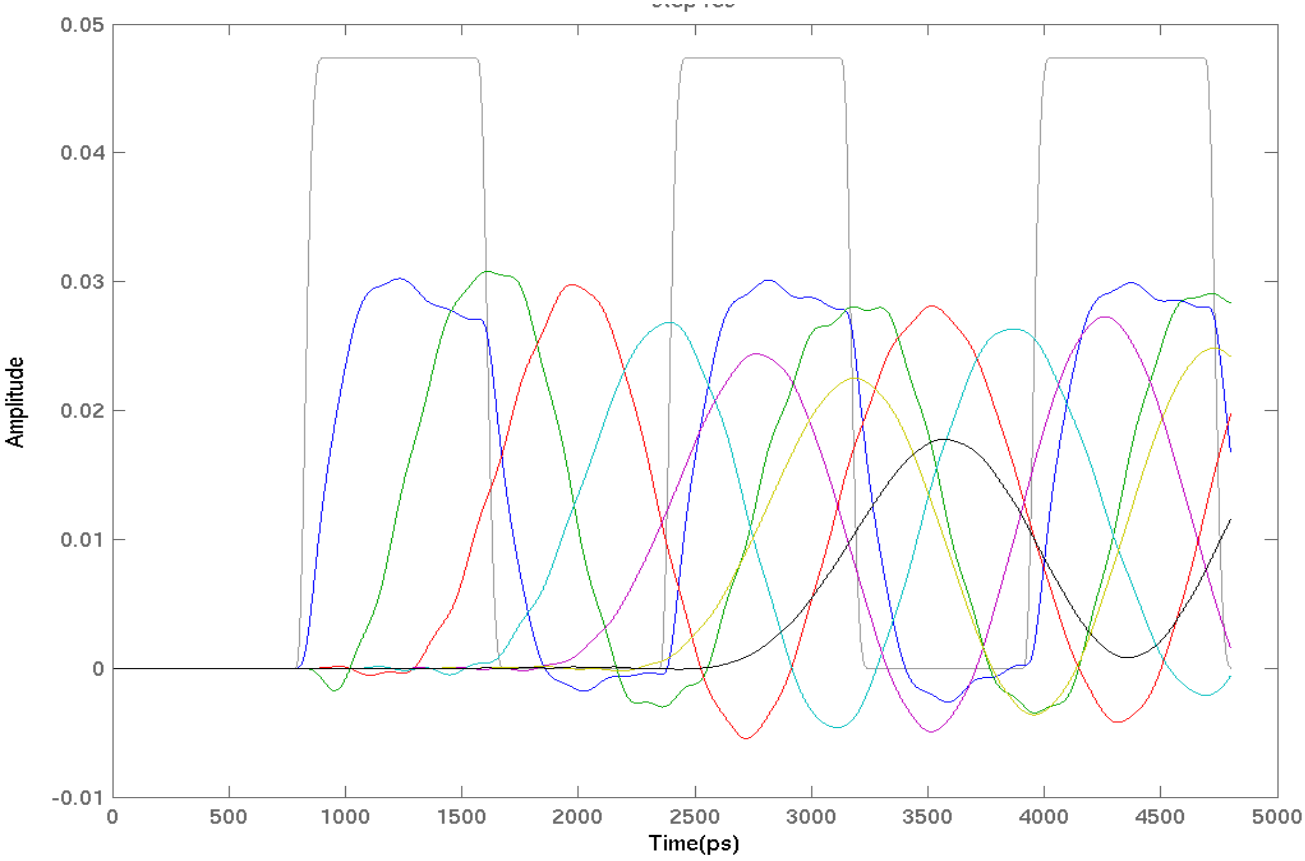
The following graphs display the matlab simulation results for the delay line.



Graph 1: group delay response



Graph 2: Magnitude response



Graph 3: Pulse response for 6.25Gb/s step input

6.2 TRASCONDUCTANCE FOR GAIN

At this high frequency, the transconductance should be as simple as possible otherwise the frequency response will be bad. So, the first choice was to use simple differential amplifier. But it have low output resistance and input and output interaction is significant.

Gilbert cell was found appropriate for this application. To decrease the input capacitance, it was tried to use a buffer but the frequency response was not too the mark.

The Gilbert cell(Fig. 16) was designed was a dc gain of one at 80C.

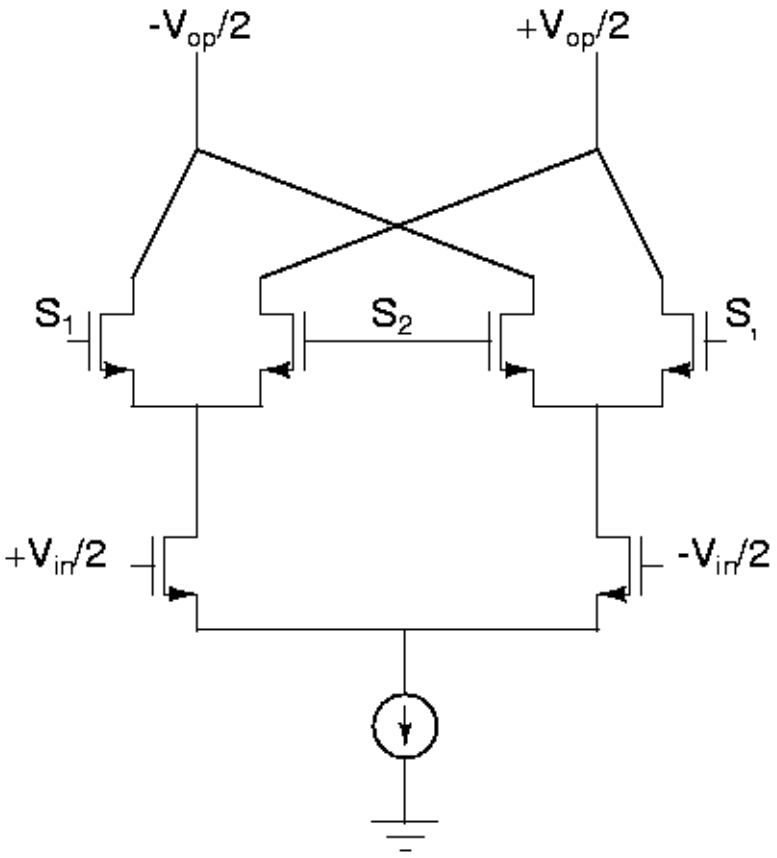


Fig. 16: Gilbert Cell

To generate the control signals S1 and S2 by using a single control signal, the circuit shown in Fig. 17 was used.

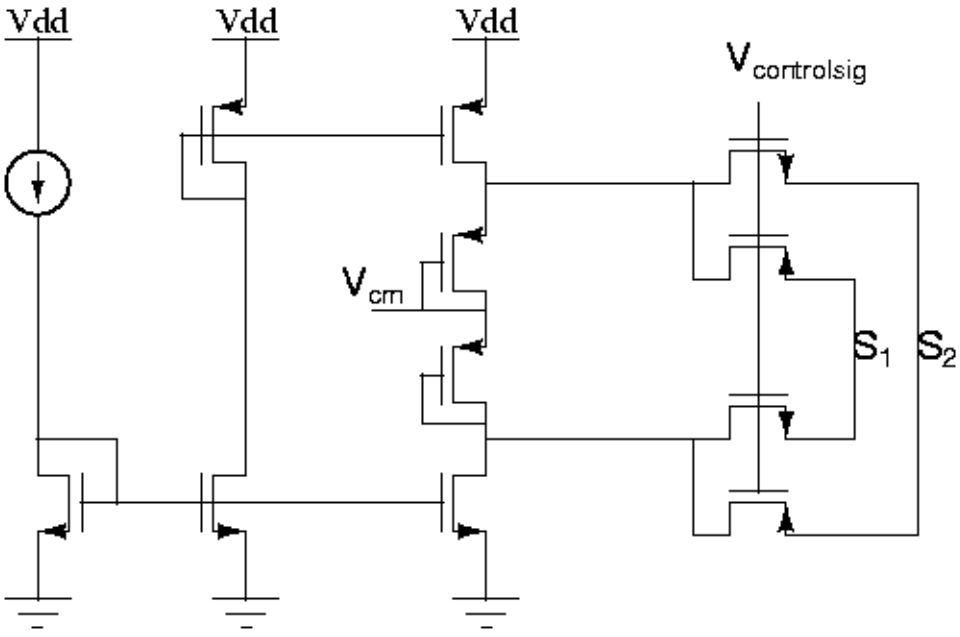


Fig. 17: Switching Circuit

6.3 INPUT TRANSCONDUCTANCE

As good ac voltage sources are not available so to facilitate efficient testing, the delay line was fed through a transconductance. Basic differential amplifier(Fig 18) was used for this application.

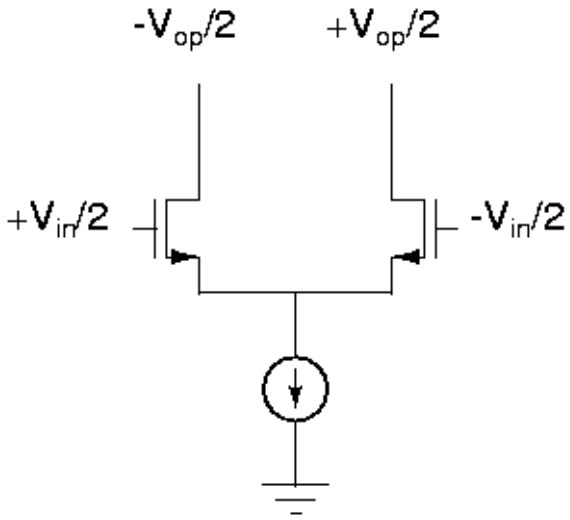


Fig. 18: Basic Differential Amplifier

6.4Layout

The size of the chip with pads is 1.5u by 2u.

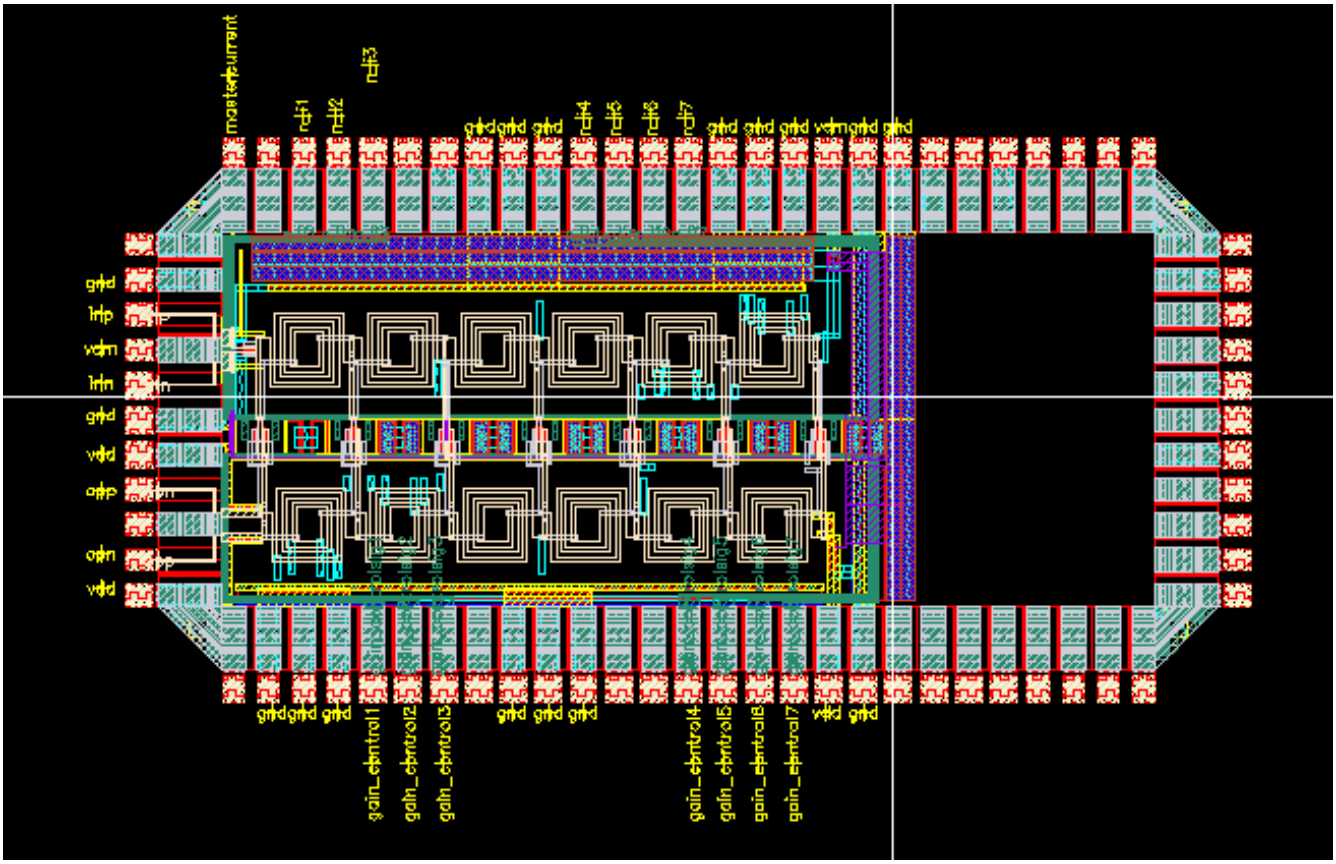
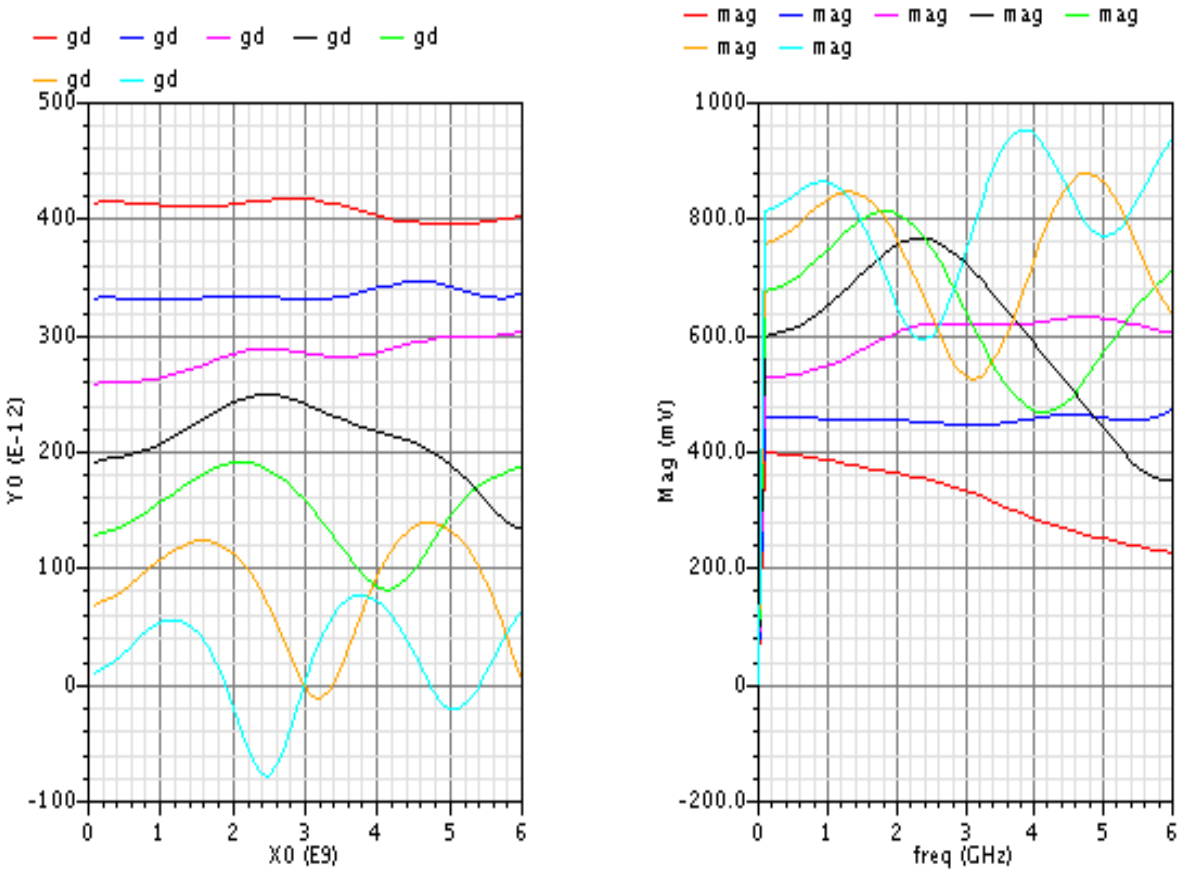


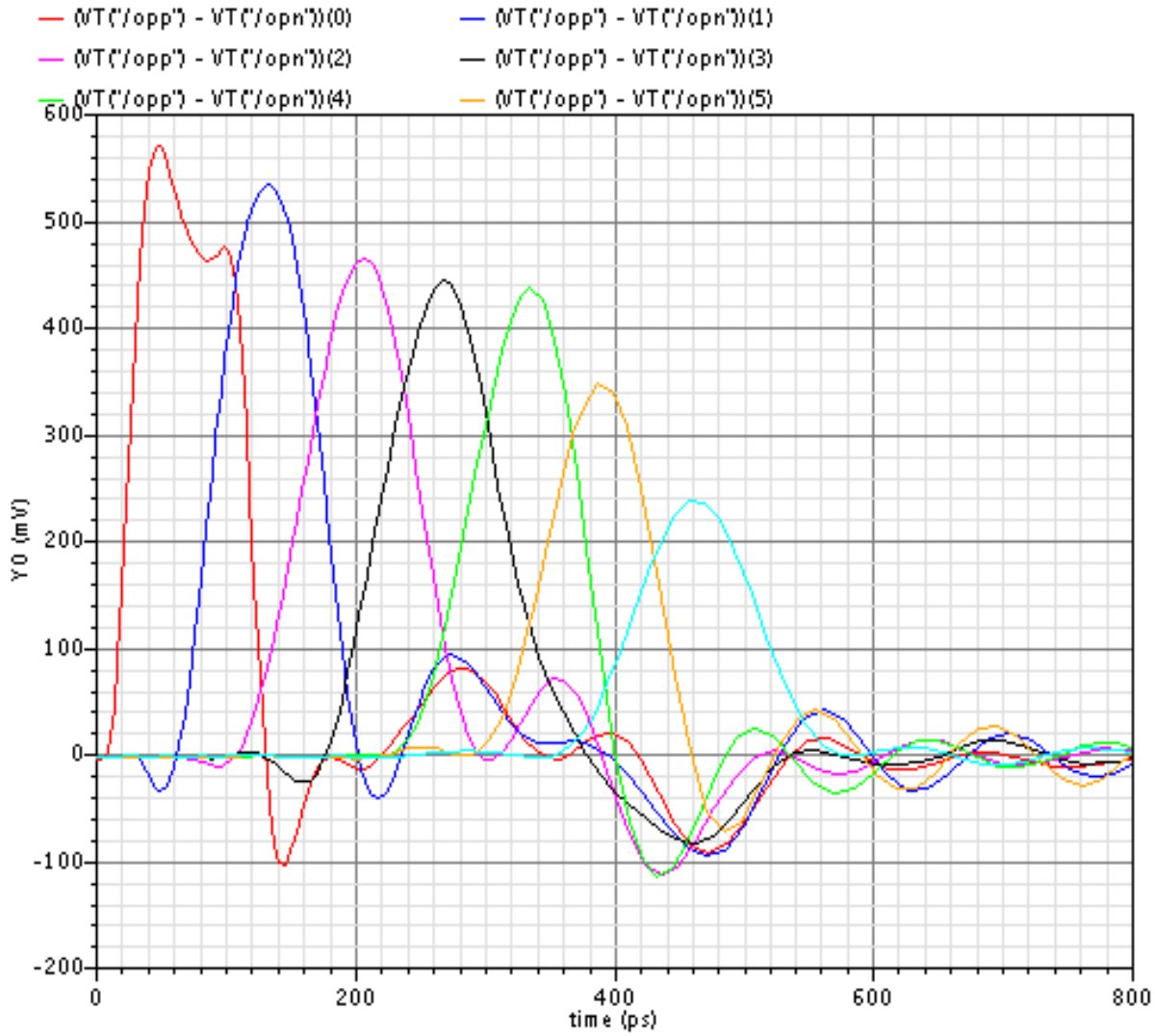
Fig. 19: Snapshot of Layout

For simulations on the extracted circuit, inductors were removed. Then the remaining circuit was extracted in CADENCE. For the inductor, a spice netlist was added. The following simulation results were obtained.

For obtaining every graph, all but one corresponding transconductance was kept on. So, zero current flows though the other trans conductances which decreases their input and output capacitance, thus effecting the response.



Graph 4: Group delay and magnitude response for the extracted circuit



Graph 5: Pulse response for a pulse of width 80ps.

7 FURTHER REDUCTION IN SIZE

The above mentioned idea for the design can further be modified to reduce the size of the delay line. In the previous idea, the inductor has been tapped at various corners to put capacitors.

In this section, it is shown that it is possible to tap the inductors at the intermediate corners to put capacitors as well as to take outputs. This idea is clearly demonstrated through Fig. 20.

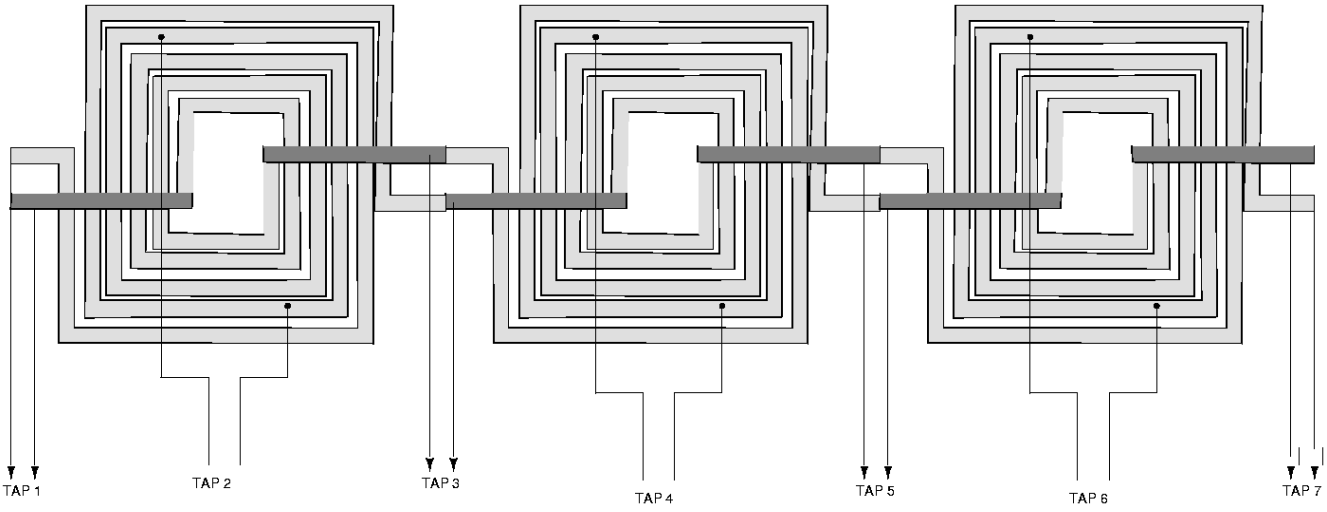


Fig 20: Tapping the inductors for output

7.1Design issues

---The question here is : where to tap for the output?

Each inductor in this case was 4.2nH non-differentially. So, the point on the inductor at which the inductance in 2.1nH non-differentially from both the end taps is the right point to take an output tap.

This should be clear by the following example(Fig. 21).

ABC forms inductor1. XYZ forms inductor2. B and Y should be chosen such that

L1+M12+M13+M14 = L2+M21+M23+M24

= L3+M31+M32+M34 = L4+M41+M42+M43

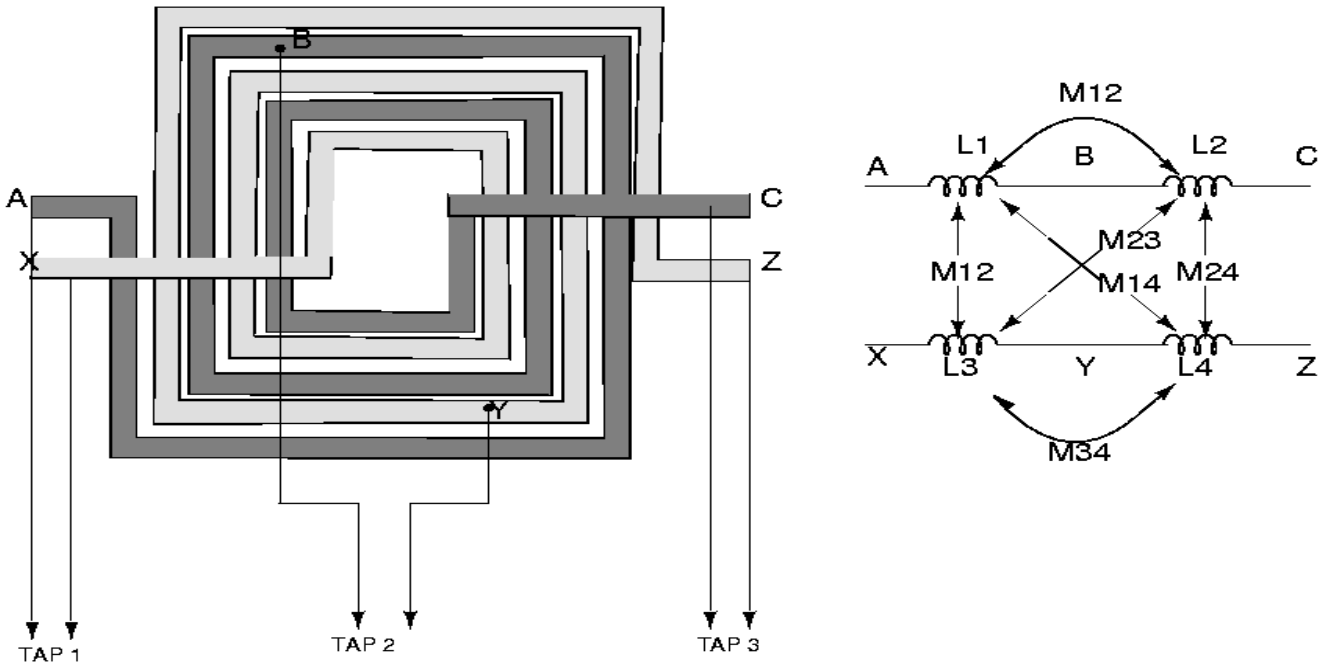


Fig. 21: Tapping the inductor for output

--- For good results, its preferable to keep the coefficient of coupling between the differential inductors under 0.6. The results shown here are for the value of 0.6.

7.2 Advantages compared to the delay line presented in chapter 6.1

-- The total resistance of delay line decreases, so the signal attenuation is reduced. Size can be further reduced by decreasing the width of the inductor segments if same amount of resistance is tolerable.

-- Inter-loop capacitance decreases so more transconductance capacitance can be tolerated.

-- Size decrease to around 70% for the same performance.

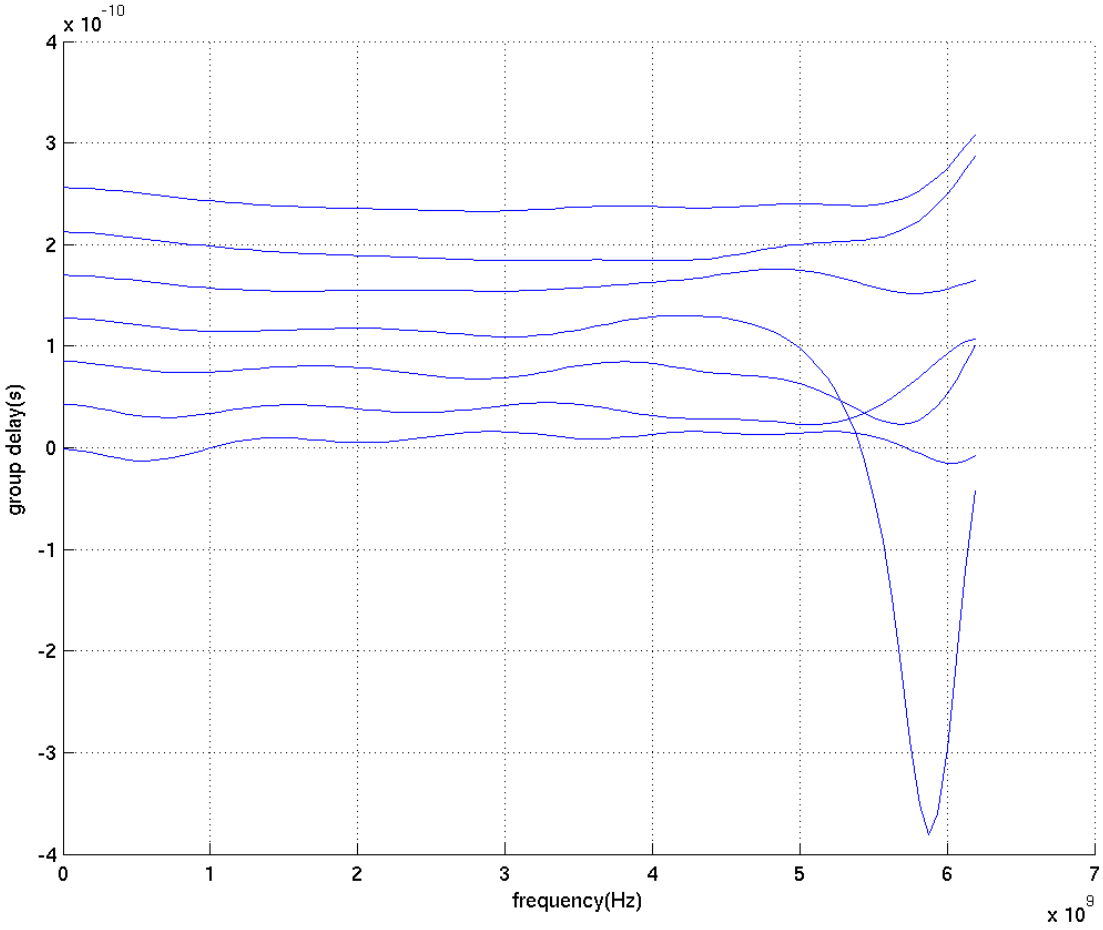
7.3 More Analysis

A even a bigger inductor of around 12nH differentially can be designed and tapped at two points to take outputs. Then only two differential inductors would be needed for the complete delay line. But then, the bandwidth to which optimization is effective goes below 5GHz (around 3GHz).

If a single inductor is wound for the complete delay line, bandwidth reduces further and so the idea becomes infeasible.

7.1Performance

After simulations in matlab, the following responses were obtained.



Graph 6: Group delay

7.2Layout

The size of the chip is 1.5u by 1.5u with pads.

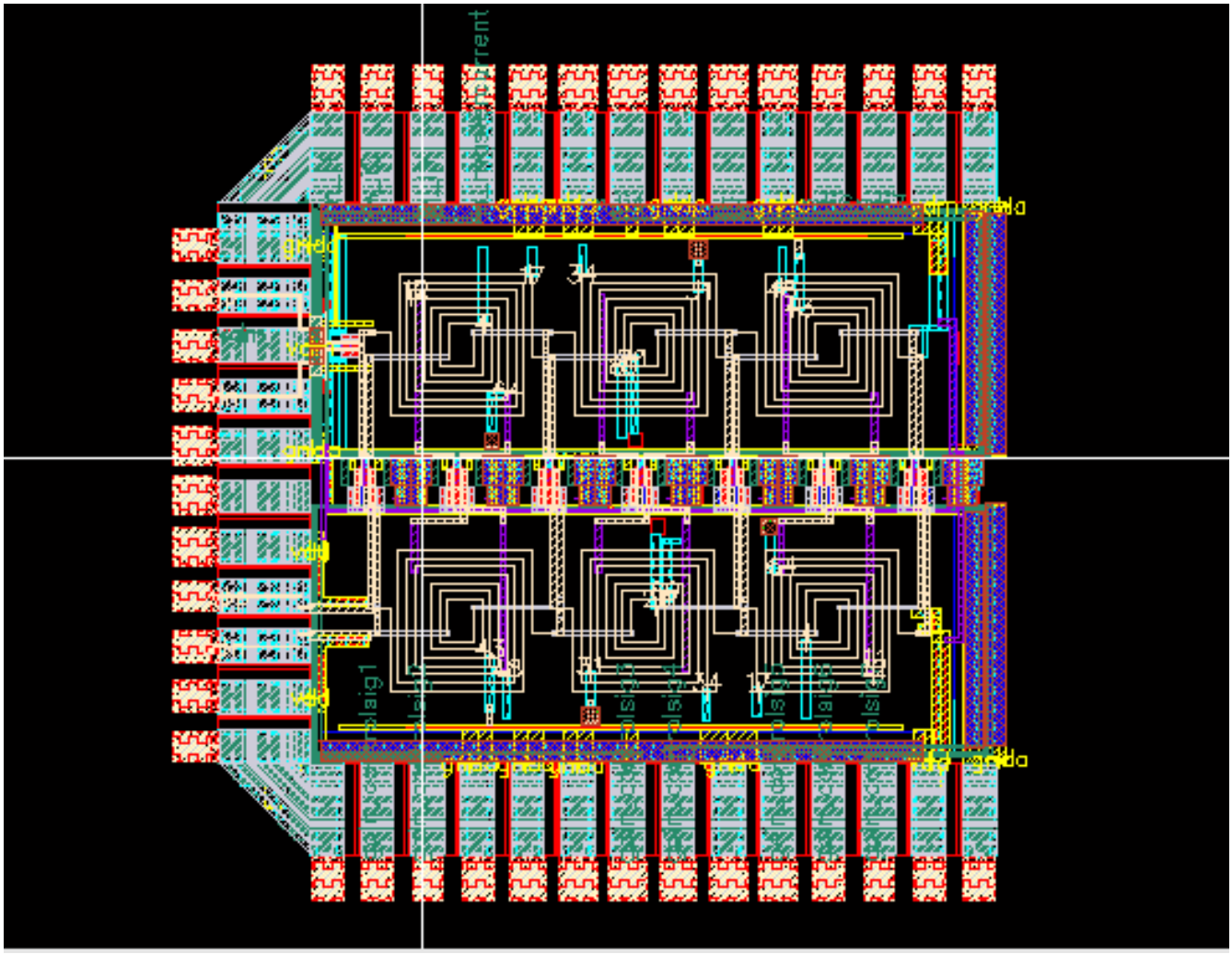


Fig 22: Layout

8. DELAY LINE WITH NO INPUT TERMINATION

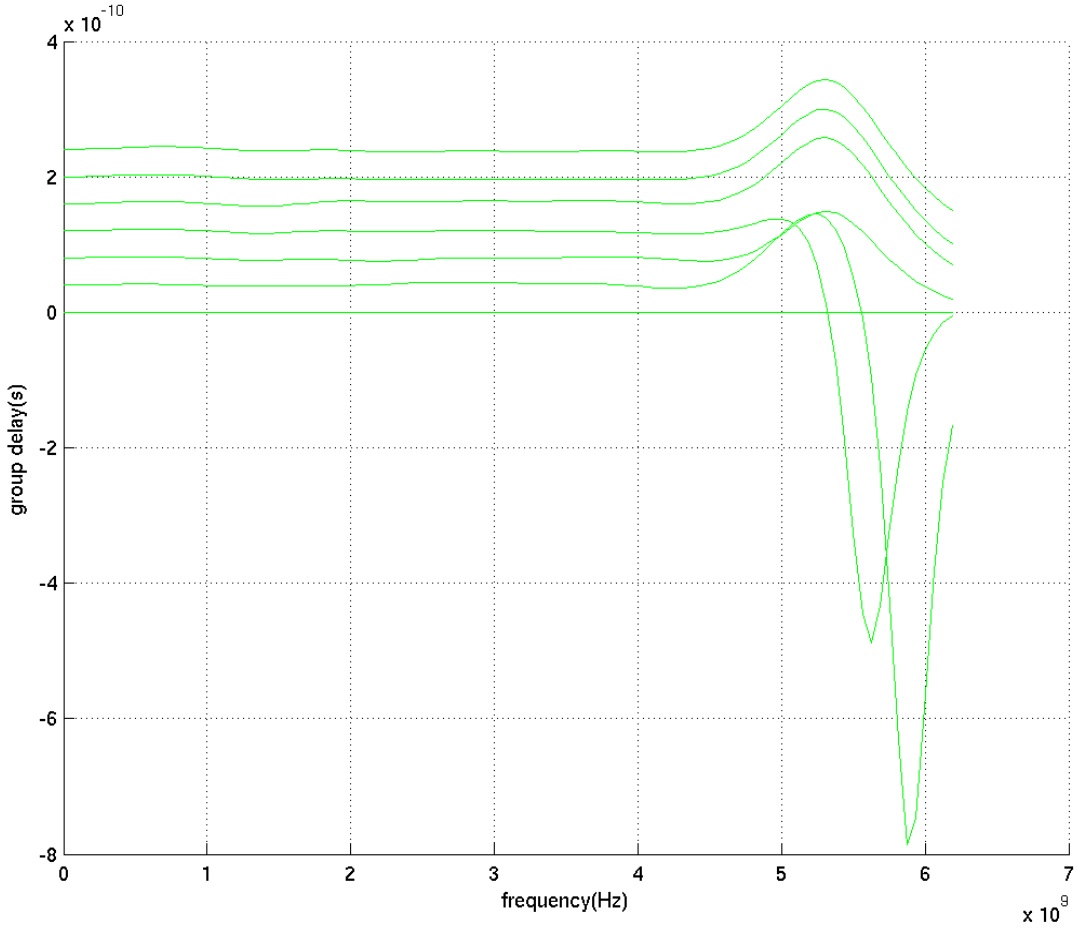
In an ideal delay line, termination at the output will be sufficient. But the conventional LC ladder delay line needs termination at both ends due to non-idealities. This has the disadvantage of signal attenuation.

This has following advantages:

1. The value of the transconductance can be decreases.
2. Due to decrease in the transconductance, the transconductance capacitance will decrease.
3. Now, more inter-loop capacitance and series resistance can be tolerated which will reduce the size of the delay line further.

Performance

Following response was obtained from matlab simulations.



Graph 7: Group Delay

9 FILTER

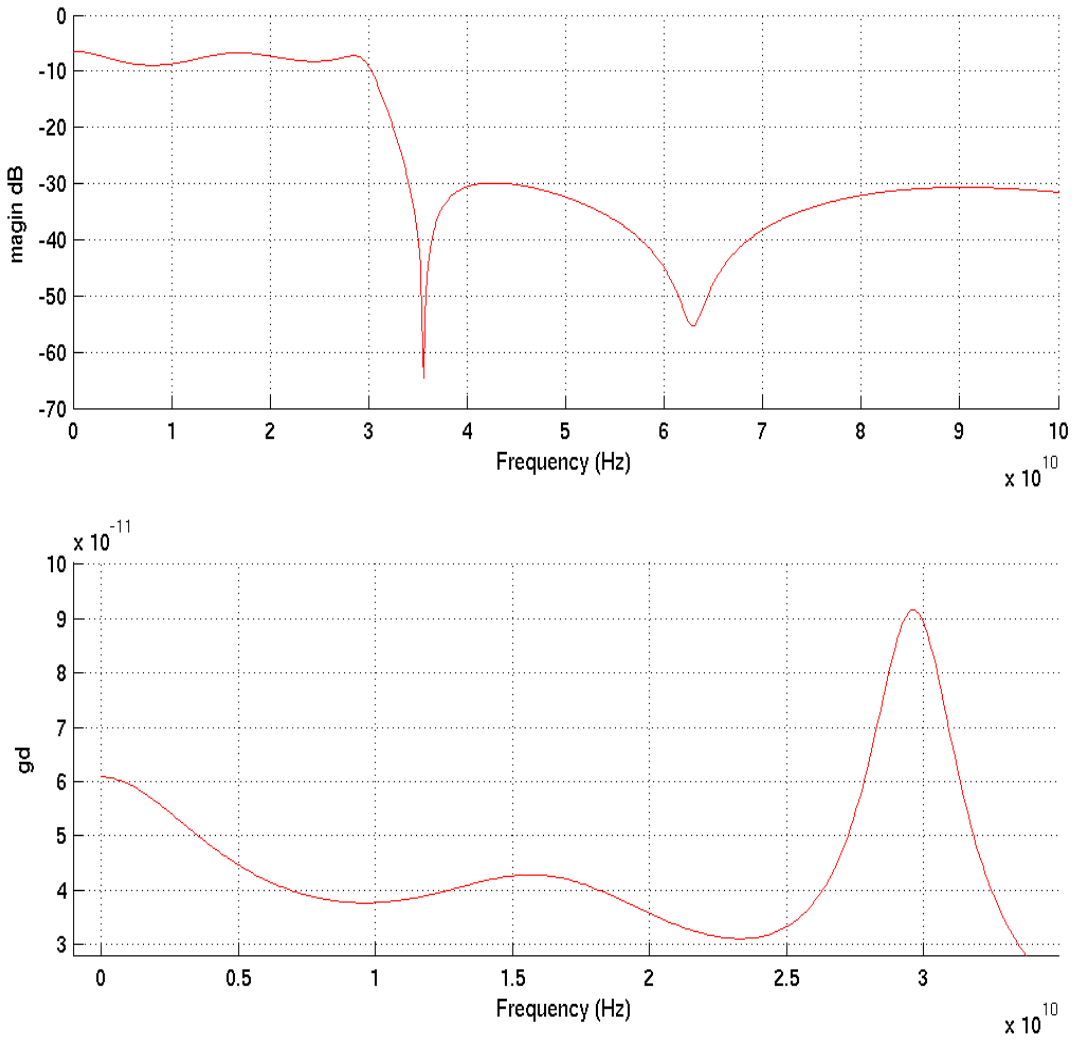
The techniques presented here for the design of delay line can also be used to design filters for RF/Microwave frequencies. There is a posibility of low pass, band pass and band stop filters. But as band pass and band stop filters demand very high Q value. On-chip inductors have a typical Q of only around 10 so it will be very difficult of design such filters with on-chip spiral inductors.

But it is practical to design low pass filters. No literature was found which talks about filter design using positive magnetic coupling. So, various optimization techniques were tried for the design. Some of the promising techniques discovered will be discussed in this report.

Method 1

Suppose a nth order low pass Bessel(say) filter has to be designed. This ideal filter will have (n-1)/2 (if n is odd) or n/2 (if n is even) number of inductors. A spiral inductor should be designed such that its value of inductance should be equal to the sum of the inductor values of all the inductors in the ideal filter. Then the capacitors at various corners of the inductor should be optimized to get the desired magnitude response.

This technique is easiest of all the following techniques but not very useful as the achievable attenuation in the stop band will not be more than 30. Graph 8 show the magmitude and group delay response of one such filter designed. It can be seen that the attenuation iin stop band is only 30dB.



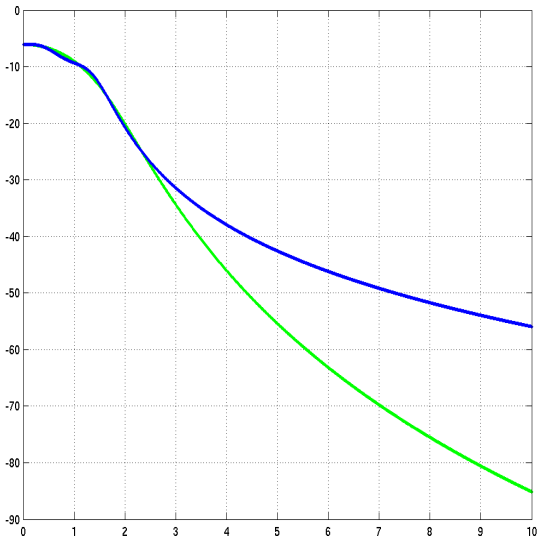
Graph 8

Method 2

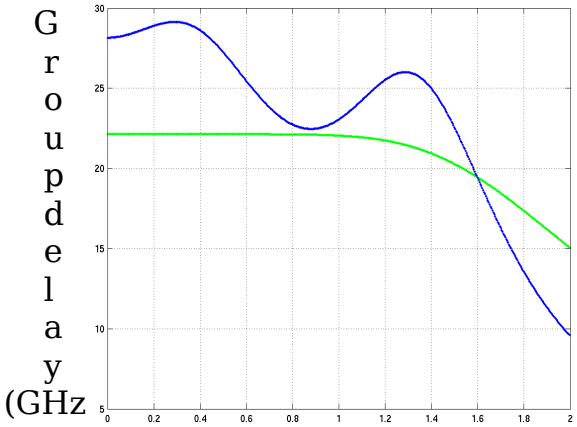
Suppose the behaviour of a 7th order bessel filter has to be mimiced, then a toplotogy as shown in fig 3(a). Will be modeled in matlab. Then the values of the inductors and the capacitors will be optimized to mimic the ideal filter response.

Both magnitude and group dealy responses can be optimized at once. But here there is a trade-off. There are three quantities here: magnitude response, group

delay and the coefficient of coupling between the inductors. If both magnitude response and the group delay are required to be veryc lose to the ideal behaviour as in graph , then the coupling coefficient between the inductors has to be below 0.2. If coupling coeficient between the inductors is as high as 0.5, then either magnitude response or group delay response will be close to the ideal filter as shown in figs 9, 10, 11.



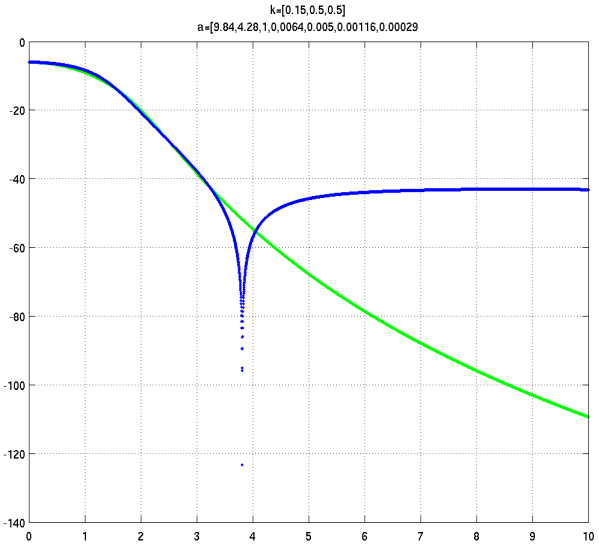
frequency(GHz)



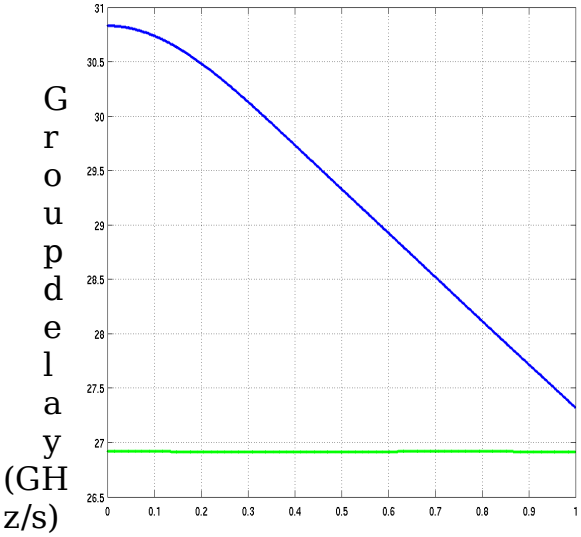
Group delay (GHz/s)

frequency(GHz)

Graph 9



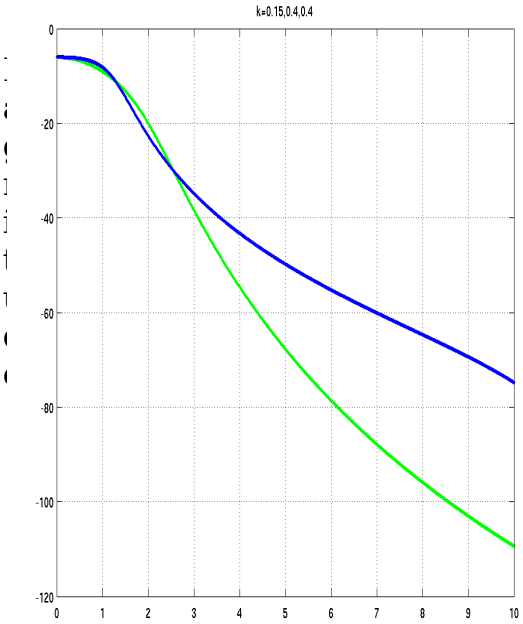
frequency(GHz)



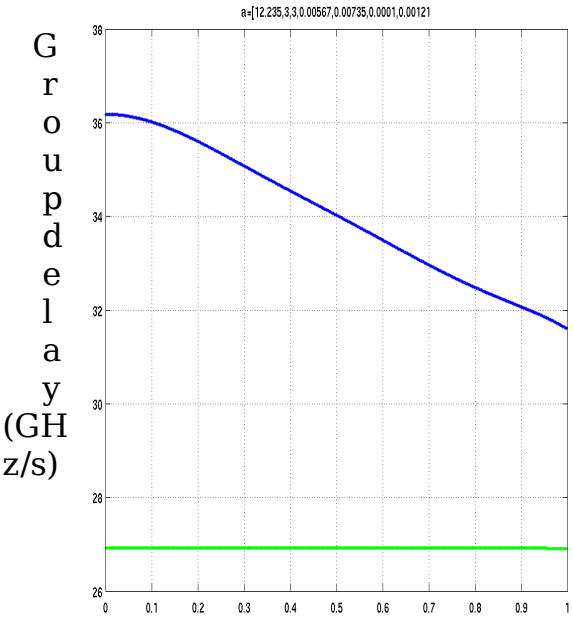
Group delay (GHz/s)

frequency(GHz)

Graph 10



frequency(GHz)



Group delay (GHz/s)

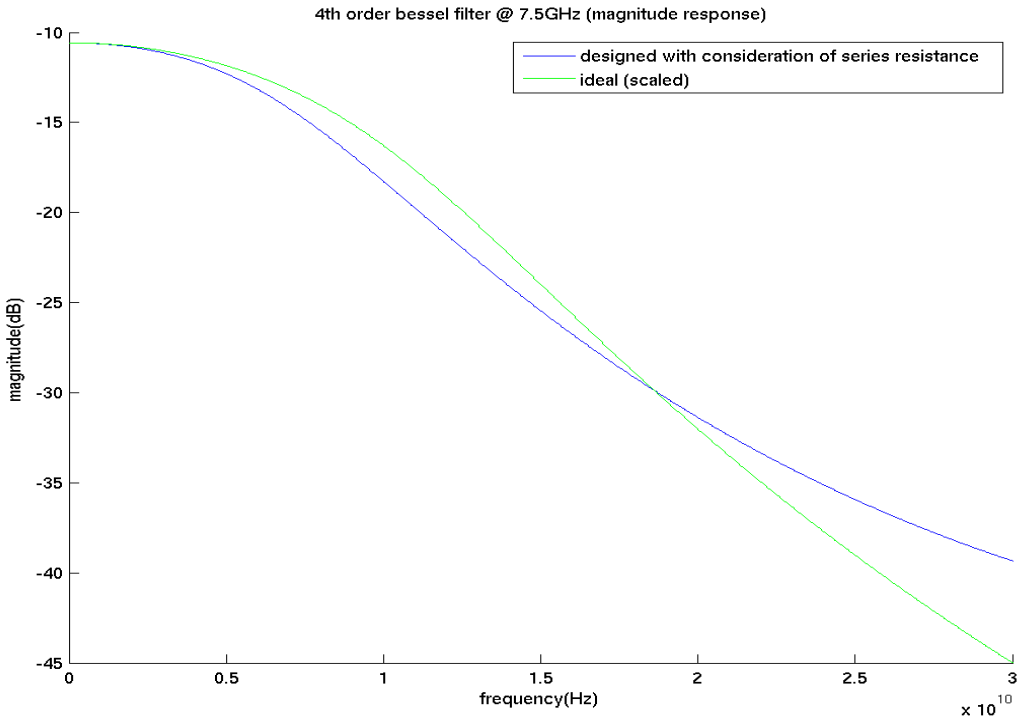
frequency(GHz)

Graph 11

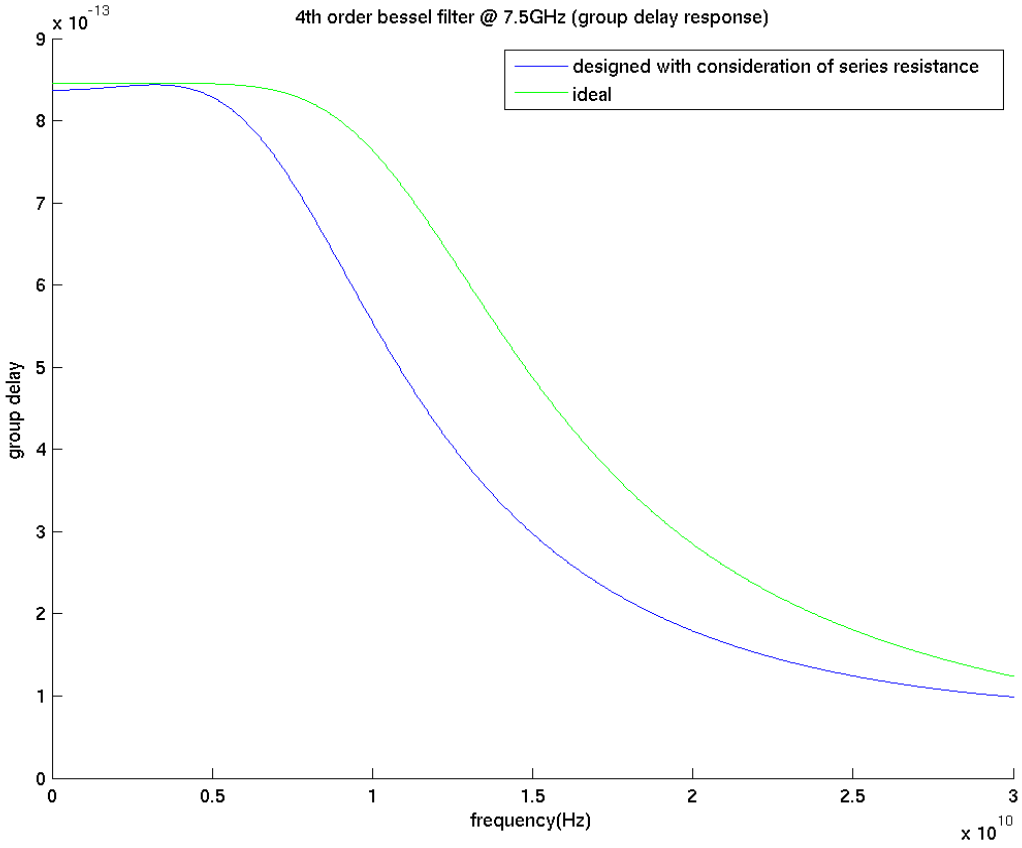
Method 3

Method 2 has two major drawbacks. Firstly, for high coupling coefficients between the inductors and a good magnitude response, group delay will not be close to the ideal filter. Secondly, series resistance of the inductor has not been taken into account.

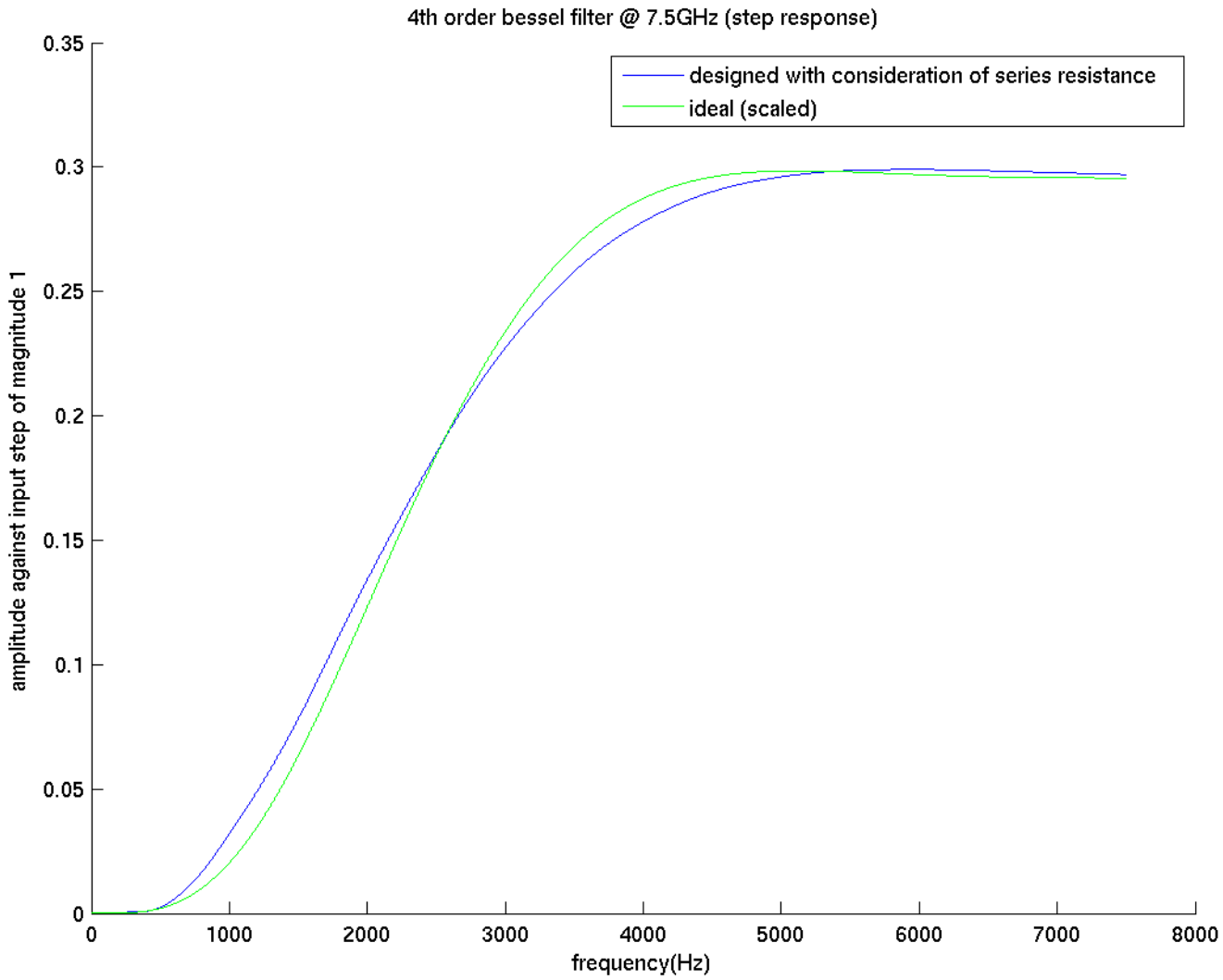
It was discovered that better optimization results are optained when optimization was run to mimic the step response of the ideal filter. To avoid the overshoot in the step response, filter should be damped by increasing the series resistance of the inductors intensionally. A response of a 4^{th} order bessel filter designed of this methodology gas been shown in fig 12, 13, 14.



Graph 12


4th order bessel filter @ 7.5GHz (group delay response)
x 10^-13
9
8
7
6
5
4
3
2
1
0
group delay
designed with consideration of series resistance
ideal
0
0.5
1
1.5
2
2.5
3
frequency(Hz)
x 10^10

Graph 13


4th order bessel filter @ 7.5GHz (step response)
designed with consideration of series resistance
ideal (scaled)
amplitude against input step of magnitude 1
frequency(Hz)
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0
1000
2000
3000
4000
5000
6000
7000
8000

Graph 14

9. FUTURE WORK

The design presented here is far from a LC ladder due to following reasons:

-- There is very strong magnetic couping between the inductors.

-- Series resistance of the inductors is high.

-- Inductance needed is more than the conventional LC ladder design.

-- The sum of the optimized capacitor is significantly different from the LC ladder design.

This design can be viewed a complex high order passive filter. So there is no reason why the total amount of inductance should be close to the LC ladder design.

If this ideal can be realized, then the size can be reduced further.

APPENDIX A

THINGS TRIED BUT DID NOT WORK

-- For good results the total inductor should be around 10% more than the conventional LC ladder. If the amount of inductance is same as the convention LC ladder, then the group delay response is flat but the value of group delay is less than required.

To solve this issue without increasing the amount of inductance, following change was made in the optimization routine.

The total mount of capacitance after optimization was observed. Now an additional constrain in optimization was put that the some of the total capacitance should be a fixed values. This fixed value was obtained by hit and trial such that the group delay at dc is as required. But now, after optimization, group delay is clearly as expected at the dc but the frequency response is bad.

-- In convention LC ladder

Following the same termination trick, the optimization was run assuming C transconductance capacitance at the middle taps and C/2 at the first and the last tap. But this does not improve or degrade the performance.

Infact the performance is same even if the terminating capacitance is more than C.

--A simpler way to design the delay line is to optimize a single inductor for delay of 40ps at the output and 0ps at the input. Then this inductor can be cascaded to form a delay line. But here the error accumulated and the performance is inferior compared to the optimization of the entire delay line.

--This technique has a constrain that the inductor can to be wound to tightly. Otherwise, the inter-inductor capacitance is too high too get a proper design. This is not a great problem from magnetic coupling point point of view. Coupling coefficient of around 0.6 can still be realizable. Anyway, even if the inductor is wound tighter, coupling will not increase above 0.75. Here it should be kept in mind that magnetic coupling changes much slower to capacitive coupling with distance.

This issue is that by winding a tighter inductor, size of the chip can be decreased further.

To solve this issue, one idea was tried. It goes like this. Two non differential delay lines were designed. The good thing is that now the inter-inductor capacitance does not contribute to the shunt capacitance. The two delay lines were placed very close to each other. They will couple now. Now the optimization was run on the complete differential line. But the obtained response was much inferior to the design presented here.

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APPENDIX B

SOFTWARE TRICKS

Fasthenry

-- A discretization of two three along the height and five along the width of the inductor is optimal. A better discretization increase the simulation time without noticeable change in accuracy.

-- It is advisable to generate a picture of fasthenry to verify the inductor.

Fastcap

-- Discretization of the ground plate is very critical for simulation time. Discretization of one should be used for the inductor segments. The discretization of the ground plate should be such that the size of each block on the ground plate is more or less the same as that on the inductor segments.

-- Clearly, there can be many choices for the discretization of the ground plate as explained above. But in some rare cases, some of these choices may take large simulation time. Then one should just make a slightly different choice for discretization of the ground plate.

-- Fastcap will give warning that some of the capacitors calculated are negative. Then the value of such capacitors should be seen. In most of the cases, magnitude of these values will be much smaller than the other values. This can be safely neglected.

-- For the ground plate, option '-p' should be used. This reduces the simulation time.

-- If very accurate results are not required, used of fastcap can be safely eliminated. Most of the technologies provide elaborate tables listing capacitance value between interconnects on all the metal layers. In in some of the cases, the use of fastcap has to be eliminated. For example, In 'UMC 180 RF/MM', the distribution of dielectric layers around the top metal layer is too complex to be simulated in fastcap.

Matlab Optimization

-- For the frequency of interest(1-10GHz), inductors are in nH and capacitors in pF. These values are very small and matlab cannot handle very high degree of transfer functions at these frequencies. So, the system should be scaled down appropriately. For circuits mentioned in this report, frequency scaling may vary typically from 1e10 to 1e13.

-- More importantly, the frequency scaling needed may vary in a single problem. For instance, suppose a optimization starts with a frequency scaling of 1e12. It may be possible that after few iterations, the frequency scaling has to be increased to 5e12(say). If this change is not done, optimization routine will apparently keep running but solution will not improve. Actually, the coefficients of the transfer function will become NAN or infinity in matlab.